New Driving Schemes of Cholesteric Liquid Crystal Display for High Speed and Uniform Gray-Scale Performance

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Zusammenfassung

Für eine lange Zeit war das Fehlen eines effektiven Treiberschemas ein Haupthindernis für die Anwendung der Cholesterischen LCDs. Viele Treiberschemata wurden in den letzten Jahren wie das herkömmliche statische Treiberschema sowie mehrere schnelle Dynamische Treiberschemata (DDS) entworfen. Diese Treiberschemata, die in Kapitel 3 eingeführt werden, zeichnen sich entweder durch gute Bildqualität oder durch schnelle Ansteuergeschwindigkeit aus. Als Verbesserung führen wir ein verbessertes dynamisches Treiberschemata (genannt Enhanced Dynamic Driving Scheme) ein, das ermöglicht, das Ch-LCD nicht nur in den Ein- oder Aus-Zustand, sondern auch in mehrere verschiedene Graustufen anzusteuern. Im Enhanced Dynamic Driving Scheme sind die Selection und Hold Wellenformen neu gestaltet, so dass Pixels auf bestimmte Reflexionen angesteuert werden können, während die nicht selektierten Pixels untangiert bleiben. Im Gegensatz zum $U/\sqrt{\frac{3}{2}}$ DDS Verfahren, das fünf Spannungen verwendet, werden nur drei Spannungen im neuen Enhanced Dynamic Driving Scheme benötigt. Die höchste Treiber-Spannung wurde um 12%, verglichen mit dem $U/\sqrt{2}$ DDS, ebenfalls reduziert. Die Ansteuergeschwindigkeit beträgt 1.2 ms / Zeile, die höher als viele dynamische Treiberschemata ist. Das Enhanced Dynamic Driving Scheme zeigt also in fast jedem Aspekt eine bessere Leistung und bessere Parameter.

Graustufen können im bistabilen Ch-LCD realisiert werden und sind eigentlich ein Mischzustand des reflektierenden planaren Zustands (planar state) und dem streuenden fokal-konischen Zustands (focal conic state). Im Enhanced Dynamic Driving Scheme, das in Kapitel 3 eingeführt wird, werden Graustufen in der Ch-LCD mit dem effektiven Wert (root of mean square RMS) der angelegten Spannung erzeugt, anstatt die Höhe der Spannung zu modulieren. Somit können Graustufen von verschiedenen RMS-Spannungen durch Verschiebung des Tastverhältnisses der ansteuernden Wellenformen erreicht werden. Die Anzahl der Spannungsquellen könnte verringert werden, so dass die Komplexität und die Kosten des Treiber deutlich reduziert werden können.

Aufgrund der intrinsischen Eigenschaften des Ch-LCD, dass der Zustandsübergang in DDS ziemlich steil ist, ist die Anzahl der Graustufen, die mit dieser Methode erzeugt wird, eher bescheiden. Um die Anzahl der Graustufen durch das Enhanced Dynamic Driving Scheme zu erhöhen, haben wir eine neue Methode, genannt Multi-Selection-Method (MSM), vorgeschlagen. Diese Methode scannt das Display zwei oder mehrere Male während eines Ansteuervorgangs. Somit kann eine Graustufe in zwei oder mehr Stufen verfeinert werden, so dass die Anzahl der Graustufen ohne erhöhte Hardwarekosten mindestens verdoppelt werden kann. Die Graustufen in dem dunklen Bereich sind auch erweitert, das die Anforderungen der nichtlinearen Gamma-Korrektur trifft. Während des Experiments wurden das Two- und das Three-Selection-Verfahren

für die Ansteuerung der Graustufen durchgeführt. Im Anbetracht der Tatsache, dass das Three- oder gar das Four-Selection-Verfahren mehr Zeit verbraucht und dafür die Anzahl der Graustufen im Vergleich mit dem Two-Selection-Verfahren nur ein wenig erhöht, wird das Two-Selection-Verfahren bevorzugt.

In Ansteuerung der Graustufen auf Ch-LCD ist die Gleichmäßigkeit der erzeugten Graustufen ein weiteres zu betrachtendes Thema. Leider ist die Gleichmäßigkeit der Graustufen, die durch ein DDS erzeugt werden, nicht zufriedenstellend, egal ob im One- oder Multi-Selektion-Verfahren. Um die Gleichmäßigkeit der Graustufen in einer hohen Ansteuergeschwindigkeit zu verbessern, schlagen wir ein schnelles statisches Treiberschema, genannt Fast Static Driving Scheme, vor, das auf dem Übergang von einem stabilen Zustand in einen anderen stabilen Zustand, aber nicht über einen meta-stabilen Zustand, basiert ist. Die erzeugten Graustufen zeigen gute Gleichmäßigkeit im Vergleich mit den von einem DDS erzeugten Graustufen. Weil der Übergang der Zustände an der linken Seite der R-V Kurve (Reflection-Voltage) geschieht, die sanfter als die rechte Seite verläuft, wird die Anzahl der Graustufen auch noch erhöht. Jedoch ist das Fast Static Driving Scheme etwa halb so schnell wie das Enhanced Dynamic Driving Scheme.

Ein weiteres Verfahren, um die Ansteuergeschwindigkeit zu erhöhen, ist das Multiline Addressing Verfahren, das für die PM-LCD und PM-OLED erprobt ist. Wellenformen für die zweizeilige Adressierung wurden für das Enhanced Dynamic Driving Scheme entworfen, um die vier Kombinationen der angesteuerten Zuständen zu erzielen. In Experimenten und Tests auf Ch-LCD Panel wurde ein gutes Ergebnis erzielt. Das Multiline Addressing Verfahren für das Ch-LCD reduziert die Ansteuerzeit um fast 50%, was für große Displays mit hoher Auflösung besonders bedeutsam ist.

Um die Treiberschemata in dieser Arbeit zu validieren, wurden vier diskrete Treiber-Platinen entworfen und hergestellt. Alle vorgeschlagenen Treiberschemata wurden auf einem 160×160 Ch-LCD (bereitgestellt von AEG MIS) durch die Treiber-Platinen ausgeführt. Ein Vertex 5 FPGA wurde als Signalgeber verwendet. Experimentale Ergebnisse zeigten eine sehr gute Übereinstimmung mit den Designzielen. Dies beweist, dass die neuen Treiberschemata in dieser Arbeit richtig und wirkungsvoll sind.

Durch die Synergie mit der etablierten LCD Technologie und anderen technischen Vorzügen ist das cholesterische LCD ein vielversprechender Kandidat für die nächste Generation der farbigen E-Paper Displays. Die höhere Ansteuergeschwindigkeit, höhere Graustufen-Auflösung, bessere Gleichmäßigkeit und einfache Treiber-Architektur kann ein wenig die Wettbewerbsfähigkeit der Ch-LCD stärken. In Kombination mit möglichen Verbesserungen in anderen Eigenschaften wie Reflexion und Farbwiedergabe etc., kann das Ch-LCD eine weit verbreitete E-Paper-Technologie werden.

Abstract

Electronic paper is a kind of display which is aimed to mimic the real paper. For the E-paper display, very low power consumption, high reflectance which is close to the real paper, fast driving speed and flexibility are expected. In recent years, many technologies such as Electrophoretic display, Electrowetting display and Cholesteric LCD etc. with different characteristics have been developed to meet the tremendous market demand.

Among these technologies, Cholesteric LCD (Ch-LCD) is expected to be a promising candidate in the next generation's e-paper displays. The Ch-LCD has not only the advantages such as low power consumption, good sunlight readability and high contrast ratio and resolution but also features the potential capability of color e-paper display without color filters. It is also compatible with the plastic substrate making the flexibility easy to be achieved.

For quite a long time, lacking of a fast and effective driving scheme for driving of the Ch-LCD is a primary limitation for the enhancement of the display's performance. Conventional static driving scheme could drive the Ch-LCD at only about 50 ms / line. This slow refresh speed makes the Ch-LCD unpractical especially when the resolution gets higher. Later, fast driving scheme such as dynamic driving scheme (DDS) making use of the fast transition from the meta-stable homeotropic state to the transient planer state was proposed. The DDS could increase the driving speed to about 2 ms / line so that the practicability is largely extended. However, despite the fact that several improved driving scheme based on the dynamic driving scheme have been published one after another, the driving speed and complexity are still not well balanced. Besides, how to generate the distinct and uniformed gray scale in a fast driving speed has not been solved yet.

In this thesis an enhanced dynamic driving scheme with the ability of driving the Ch-LCD not only into the on-off state but also into several distinct gray scales at about 1.2 ms / line has been proposed. In this driving scheme, the waveform patterns are newly designed to ensure that pixels could be driven to certain reflectance while the unselected pixels remain unaffected. Gray scales are created by controlling the root of mean square (RMS) value of the applied voltages. There are only three voltage sources needed in the whole driving scheme which is fewer than that of other DDS schemes. The highest voltage used in the enhanced DDS was reduced by 12% comparing with the $U / \sqrt{2}$ DDS. The enhanced DDS has been executed on a 160×160 Ch-LCD provided by AEG MIS. Binary image with good quality has been achieved.

In the enhanced DDS proposed, the number of gray scale is limited. This is due to the steep transition at the right side of the R-V curve narrowing the space of gray scale's generation. A method called as multi-selection method (MSM) was proposed for the first time to enlarge the gray scale number. The MSM is based on two or more selections in the whole driving scheme. Thus,

the gray scales will be created in two or more steps. This method could effectively double the gray scale number and the gray scales in the dark side were extended which is consistent with the non-linear requirement of the gamma correction.

By testing this enhanced DDS, we also found that the generated gray scales are not so satisfactory in terms of uniformity. This is caused by the state transition mechanism in DDS that the stable state is achieved through the meta-stable homeotropic state and transient planer state. In order to achieve uniform gray scales we proposed a new driving scheme named novel fast static driving scheme. Gray scales in this new driving scheme are created from the stable planer state instead of the meta-stable states as in DDS. The transition happens at the smooth left side of the R-V curve. The uniformity of the gray scales is much better compared with those created by the DDS. Driving speed as fast as 2 ms / line was also achieved which is comparable with most of the DDS. Gray scale number was increased at the same time due to the smoother transition of the left side R-V curve.

Similar to the multiline driving method used in the PM-LCD and PM-OLED, we also proposed a multiline driving scheme incorporated in the enhanced DDS. Newly designed waveform pattern allows two Ch-LCD lines to be selected at the same time, which will further increase the driving speed.

Experiments were executed to validate the new driving schemes. A discrete driver system including high-voltage and analog circuit board as well as a Vertex 5 FPGA for patter generation has been designed and built. The 160×160 Ch-LCD panel was used in experiments. For the contrast ratio and gray scale's measurement, a reflectance measurement set was developed and made. Visual results were the base for the various developments and improvements in this thesis. The analysis showed that the visual results are consistent with the expectation. The two new driving schemes allow relatively high refresh time, while reasonable gray scales are achieved. Furthermore, the novel fast static driving scheme produces uniform gray scales.

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1. Electronic Paper Display Technology

1.1 Introduction

Electronic display is one of the most important links of input/output device for the interaction between human and computer or other machines. It has the ability to switch the electronic signals into readable information, such as character, number or image etc. After the first CRT (Cathode Ray Tube) display was made in 1922, many display technologies have been developed. Since the early 1970s LC (Liquid Crystal) display appeared, along with years of constant research and improvement, the LCD gradually replaces the CRT in the display area in the new era. Today the LCD is still the dominant display technology used in almost all application fields. Recently, a promising display called OLED (Organic Light Emitting Diode) is attracting attention. The OLED has some advantages even comparing with the current LCD in the aspects such as color gamut, wide viewing angle, high speed and power consumption [1].

Different from the displays being mentioned above, a novel display name electronic paper was first developed by Xerox's Palo Alto Research Center in United States in 1975. It uses charged polyethylene spheres suspending in oil bubbles which can be controlled by voltages. In 1996, MIT Media Lab successfully produces the first electronic paper display. In 2000, the first flexible e-paper display was officially presented by the American company E-ink and two years later the first color e-paper display was published in Tokyo [2]. From this point on, many technologies have been developed targeting on better solution.

The electronic paper display (EPD) is designed to mimic the visual effect of the character appearance of ordinary ink on a real paper. Unlike the conventional liquid crystal display, EPD is a bi-stable display in which the information can be maintained either without using electronic or magnetic field or at a negligible amount. It only consumes power if the content of the display is updated. Considering the slow progress of the battery technology, low power consumption is especially valuable for portable devices, such as electronic books or newspapers. The electronic paper display doesn’t require a backlight due to its capability of controllable reflection of the ambient light. It is also convenient to be made on a plastic or some kind of organic substrate which will make the display flexible.

Once the image on the electronic paper has been set, it remains for several weeks or even months after the power has been removed. This feature makes it to an ideal candidate for display applications which do not need to be refreshed frequently, for example, electronic books or billboard. Because of the extremely low power consumption, in some outdoor applications, the power of the display could be provided by the solar cell and the information as well as the instruction could be transmitted by remote site which will make it location free [3]. However, current electronic paper displays have disadvantages such as color reproduction, refresh speed, etc.

These shortcomings demand further improvements of the display technology and give topics to be researched [4].

Many technologies of electronic paper display have been developed to fulfill the tremendous market demand, such as electrophoretic display, electrowetting display and cholesteric display, etc. Each technology has its own advantages and disadvantages. [5] At least till now, not a single technology fulfills all of the requirements and strictly dominates the rest. Therefore in the field of electronic paper, these different technologies are actually racing versus each other. In this chapter, we will briefly introduce several mainstream electronic paper technologies.

1.2 Electrophoretic Display

1.2.1 E-Ink Technology

Electrophoretic is the most popular electronic paper technology today. About 90% of the commercial electronic paper devices adopt this technology. Such as Amazon's kindle e-book, Sony e-book reader and iRex reader. There are two main technologies by adopting the electrophoretic theory, which are E-ink's e-ink pearl and Bridgestone's QR-LPD. The basic schematic diagram which illustrates the working principle of the E-ink technology is shown in Figure 1-1.

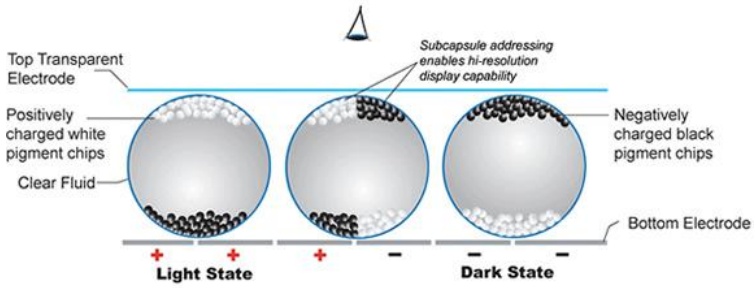


Fig. 1-1 Schematic diagram of the E-ink technology for the E-paper reader (Source: E ink Corp).

The E-ink display was proposed by the MIT Media Lab and commercialized by the company named E-ink which was spun off from MIT. Unlike the liquid crystal display, the e-ink display is made up of many small capsules, each with the diameter of around 0.04mm. The charged black and white titanium dioxide particles which are nearly one micrometer in diameter are suspended in oil and can be controlled by the applied voltage. Figure 1-1 shows the schematic diagram of how the e-ink display works. As shown in Figure 1-1, the black and white color particles are suspended in oil. By applying voltage to the transparent electrode, the charged black and white particles can be moved to the top of the capsule either completely or partly and display so the black, white or gray. A similar technology was also developed by the company Sipix by using a bigger micro-cup at a

diameter of 0.15mm.

The E-ink display could mimic the real paper vividly among today's e-paper technologies. It also features such as low production cost and high reflectance. However, the refresh speed of e-ink is low. Usually it takes 0.5 s to 1 s to refresh. In the new generation of the e-ink display, active matrix and color filters have been adopted to refresh the display at a higher speed. Video content can also be displayed fluently and consequently ends up with high power consumption. [6]

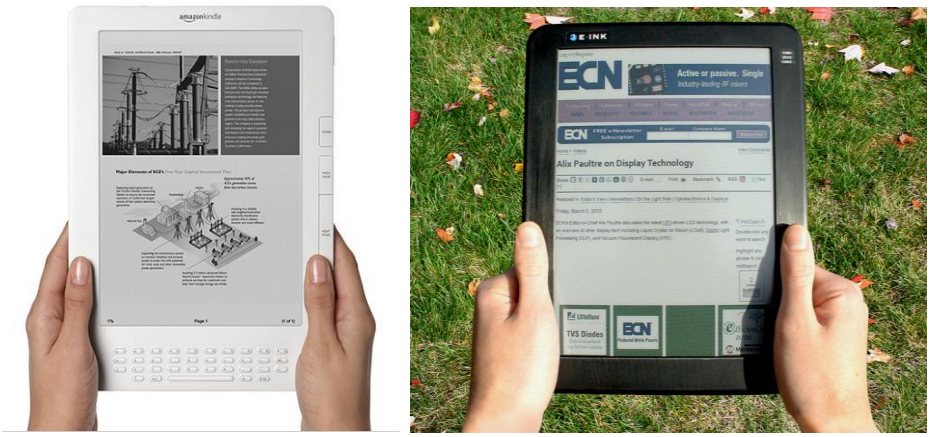


Fig. 1-2 Monochromatic and color e ink reader

Figure 1-2 shows the monochromatic E-book produced by Amazon and the color E-book by E-Ink. Both use the E-Ink's technology.

1.2.2 QR-LPD (Quick Response Liquid Powder Display)

Another approach of the electrophoretic display is the QR-LPD (Quick Response Liquid Powder Display) developed by Bridgestone and Delta. Instead of moving particles in oil as achieved by E-ink, in the QR-LPD, charged particles are moved in the air. Thus the response time will be significantly shortened comparing with the E-Ink, normally a switching from black to write takes only 0.2 milliseconds. But the QR-LPD demands higher voltages to drive the particles so that the power consumption is higher than the e ink display. Passive matrix driving is feasible in the commercial application due to the fast switching speed, which cuts production cost. Besides, since the particles are moving in the air, the QR-LPD could be used in the cold outdoor environment. Figure 1-3 shows the particle structure of the QR-LPD pixel in two states.

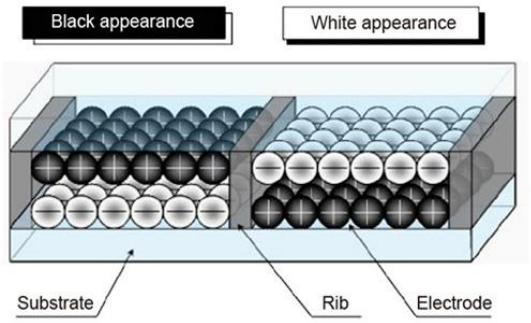


Fig. 1-3 Structure of the QR-LPD

The color QR-LPD could be made by using different powders to reflect light. Such technology was used in Bridgestone's Aerobee display. The QR-LPD could achieve high driving speed comparing with other electrophoretic displays which was previously supposed to be the most promising e-paper candidate. However, shortcomings such as high production cost etc. have forced Bridgestone to stop the research and development of this technology.

Figure 1-4 below is a picture showing the color QR-LPD made by Delta. Good viewing angle and color reproduction have been achieved as we can see in this figure.

Fig. 1-4 Delta Color e-reader using Bridgestone's QR-LPD

1.3 Electrowetting Display

As a subject of the Nature in 2003, Philips proposed a video speed electronic paper display named electrowetting display (EWD). The EWD could be operated in several modes including reflective, transmissive and transflective as well as enabling the color video with a response time 70 times than the current reflective display making it a high potential candidate for the future's color

electronic paper. It also allows applications of large scale displays such as TV based on the conventional manufacturing processes.

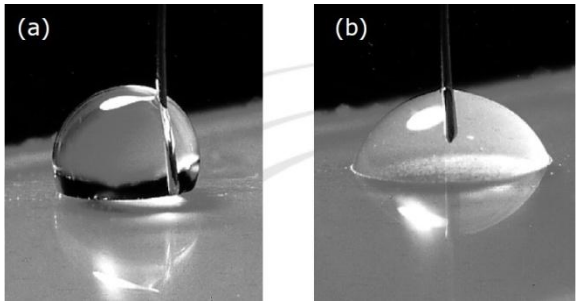


Fig. 1-5 Cross-section of the EWD

Figure 1-5 is an example to show the liquid shaped by the electric field. The switching between the two shapes could be very fast leading to fast driving speed. The Electrowetting is based on the microfluidic phenomena. It involves modifying the surface tension of liquids on a solid surface using a voltage. By applying a voltage, the wetting properties of a hydrophobis surface can be modified and the surface becomes increasingly hydrophilic. [7]

With Electrowetting displays, surface tension of colored oil is used for image display. Applied electric field could force the oil to disperse leading to a color pixel. On the other side, the charged oil could also contract as a transparent pixel. [7]

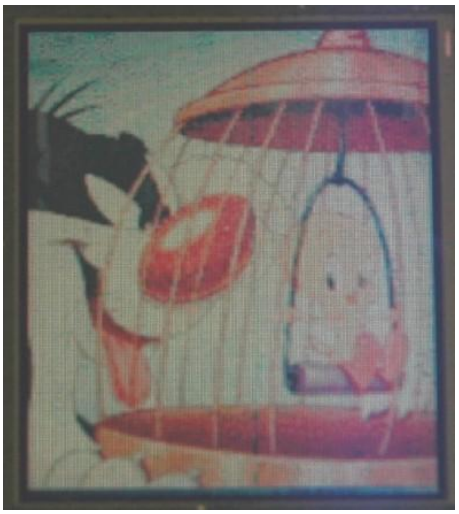


Fig. 1-6 AM-EWD made by Liquivista

Figure 1-6 is the example to show the color active matrix electrowetting display made by Liquivista. It could be observed that the resolution is quite low in the demo display. This kind of technology is still under progress now. No commercial product is available yet. [7]

1.4 Cholesteric Liquid Crystal Display

The cholesteric liquid crystal display is one of the promising e-paper technologies developed by Fujistu. Since it is one of the liquid crystal displays, it presents no obstacle to achieve the high resolution by using the mature LCD manufacturing process. Recently, the so called R2R (Roll to Roll) process has been introduced in the production of the cholesteric LCD to cut the cost. [8] This display consumes absolutely no power at the stable state and the image created on it could last for several months. This characteristic makes it a promising candidate in the applications such as electronic book, e-tag and electronic billboard etc. The cholesteric LCD also features good sun light readability as well as high contrast ratio. Besides, one of the biggest advantages of this display is that the cholesteric material could achieve different colors by adding certain dopant. Therefore the color display could be easily made without any color filter making it competitive in next generation's color e-papers. It also could be made in the soft plastic substrate making it flexible. Figure 1-7 shows a flexible cholesteric LCD made by ITRI[1].

Fig. 1-7 Flexible Ch-LCD made by ITRI

As Figure 1-7 may indicate, the cholesteric LCD could be manufactured at large scale by using the economic R2R process. This also makes the cholesteric LCD advantageous in the application where large size panel is needed, for instance, outdoor poster. [9]

In the electronic book market, Fujistu is the leading company in developing the choltesteric LCD readers. Figure 1-8 shows the newest color cholesteric e-book published by Fujistu.

[1] Flexible Ch-LCD made by ITRI using R2R process

Fig. 1-8 Fujitsu new FLEpia Ch-LCD color e book (8 inch, 4096 colors)

The color Ch-LCD E-Book as shown in Figure 1-8[2] has an 8 inch display with 4096 colors. In 2011 it was presented as the new generation FLEpia cholesteric LCD e-book featuring high brightness and rich colors. The FLEpia is made by stacking three cholesteric layers together to display color. The ambient light will be reflected in every layer to achieve three color primaries. As a counterpart, the IRTI from Taiwan also develops color cholesteric display with just one layer. The R, G and B sub-pixels are put in one and the same layer as the pixels arranged in the OLED. The color sub-pixels are made in one pixel on the plastic substrate.

Fig. 1-9 10.4 inch QVGA single layer color Ch-LCD by ITRI

Figure 1-9 shows the single layer color Ch-LCD made by IRTI[3]. The single layer color Ch-LCD

2 Ch-LCD E-book made by Fujistu. The picture could be found at: http://www.slashgear.com/slashgear-morning-wrap-up-july-12-2011-12164585.

3 Color Ch-LCD maded by ITRI; Taiwan. It was illustrated on the web page: http://www.itri.org.tw/eng/econtent/research/research03_02.aspx?sid=23

could be made using the economical R2R process for reducing the production cost. In addition, one layer color Ch-LCD doesn't have the optical interference problem which exists in the three layer's color Ch-LCD. [10]

The cholesteric LCD is a reflective display with bi-stability. There is no need for color filter and backlight. Due to its favorable features, cholesteric LCD is expected to be a promising candidate for the next generation of e-paper application. Despite the numerous advantages, it also has its drawbacks. The contrast ratio of this kind of display should be improved. Besides, how to create enough number of gray scales with good uniformity in a fast driving scheme still remains a challenging topic. The cholesteric material is sensitive to the temperature. So in the real operation, in particular the outdoor's application, the temperature compensation circuits are usually needed.

1.5 Other E-paper Technologies

1.5.1 Electrofluidic Display

Similar to the electrowetting display, the pigment colorant which used for the printing industry were put behind the pixel surface in the electrofluidic display. Inside the display pixel, a tiny reservoir takes around 5% to 10% area of the pixel is made. The applied electric field could force the liquid into the reservoir leading to a transparent pixel.

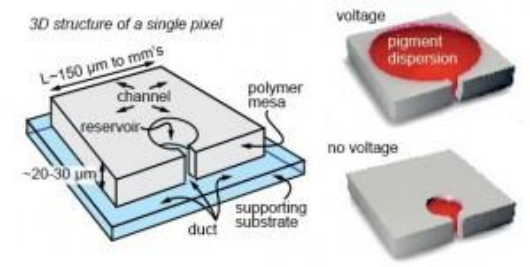


Fig. 1-10 Pixel structure of the electrofluidic display

Figure 1-10 shows the pixel structure of the electrofluidic display. The applied voltage filed would force the color pigment out of the receiver and to disperse on the pixel's surface leading to a color pixel. After the voltage was removed, color pigment will back to the receiver as a transparent pixel.

Full color electrofluidic display technology may update the knowledge of the display industry to create reflective color. Two versions of the technology are under development. The first version provides full color operation at more than 50% brightness. The second version is projected to provide even greater color performance on-par with printed office documents. [11]

1.5.2 Electrochromic Display

The chromic material was first reported in 1969. Since then, many chromic materials have been reported which have the ability to change their color reversibly when they are applied by different voltages. Figure 1-11 shows a sample of electrochromic display made by Ricoh.

Fig. 1-11 Electrochromic display (LTPS TFT 240*320)

The technology to make a working electrochromic cell is much analogous to the technology used in LCD displays. One way to make a working cell is by placing the electrochromic material between two transparent electrodes (preferentially Indium Tin Oxide, better known as ITO). The color of the EC-material is a result of changing the potential of the cell by charging the electrodes. Some recent researches show that some of the chromic materials could switch between several colors depending on the different external voltages and it is also possible to achieve the basic color in one pixel. [12]

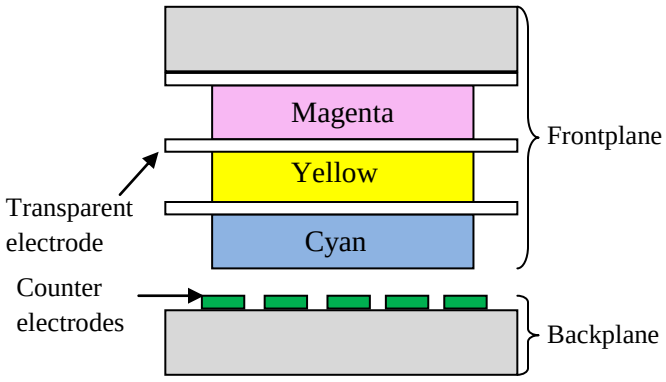


Fig. 1-12 3 Layers structure of the electrochromic device

The electrochromic display has numerous merits. First of all is the low power consumption. Similar

to many other the e-paper technology, the electrochromic display consumes power only when the content is refreshed. In the past, the driving of the display was troubled by the slow driving speed of switching the pixel from transparent state. In the new generation's EC display, this has been solved by adding porous electrodes. Typical switching times are now within the range of 200 milliseconds. The color display is easy to make without color filters. As shown in Figure 1-12, a molecular dye has been developed which can display red, green or blue, depending upon the applied voltage. This implies that no color filter usage is necessary, which diminish the brightness of the display. As to the mass production, the EC display also has a set of benefits. Recent studies show that existing LCD-manufacturers could easily transform their assembling machines to produce EC displays.

1.5.3 IMOD (Interferometric Modulator Display)

IMOD is a MEMS (Micro Electro-Mechanical Systems) based display developed by Qualcomm in USA. This display makes use of the technology named interferometric modulator to reflect specific wavelength of light to create different colors which has the same function as the color in the wing of a butterfly. The IMOD display is also bi-stable. Comparing to the LCD or OLED, the IMOD could reduce the power consumption largely, and color filter is also not needed for color display.

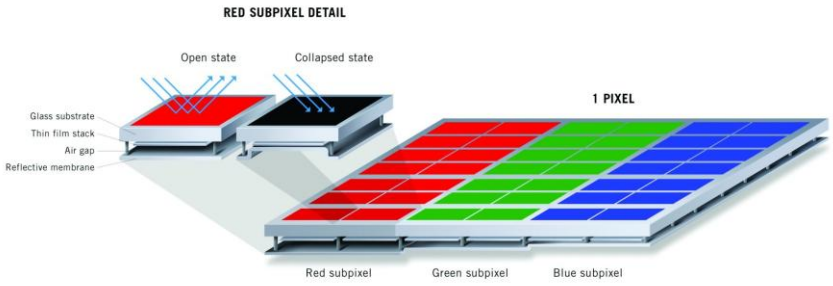


Fig. 1-13 Sample of IMOD pixel matrix

Figure 1-13 shows a sample of the pixel matrix of the IMOD. As shown in Figure 1-13, color pixel could be generated by different pixel's reflectance which could be achieved by varying the depth of the cavity. Black pixel could be achieved by shifting the back plane which will lead to an ultraviolent reflectance. [13]

Fig. 1-14 IMOD display by Qualcomm (5.7" XGA format (1024 x 768 pixels))

Figure 1-14 above shows the IMOD branded Mirasol made by Qualcomm. It could operate at 30 fps which allows a video speed application. In case of displaying video content, the Mirasol display consumes about 20% less power than the E-ink display. It also supports wide range of working temperatures. Because it is a MEMS based display, the temperature could vary between -30 ℃ and +70 ℃, allowing a wide range of environment. The IMOD is still under intensive research but it is already expected to be a promising candidate in the next generation's e-paper display to compete with the E-ink technology. The production cost of this kind of display still remains high. Cutting production cost could be possible if the production could be compatible with process of the flat panel display.

However, The IMOD display currently still has deficiencies, such as small viewing angle and low color reproduction. Comparing with e-ink's technology, the viewing experience of the display is more like the LCD but not the real paper. In SID 2012, Qualcomm has shown some of devices using the Mirasol display such as e-book and smart phone with good quality by eye observation. This kind of display may have potential value in the e-paper market in the near future.

1.6 Conclusion

In this chapter we introduced several main technologies of the electronic paper display. As a summary, the table below compares the advantages and challenges of these technologies as well as the R&D facilities.

	R&D	Advantages	Challenges
EPD **(Electrophoretic)** **(E-Ink;QR-LPD)**	**E-ink(PVI)** **Sipix** **Bridgestone**	**Mainstream technology in current e-book product (Commercialization)** **Anti-press capability**	**Hard to make color display** **color filter needed**
EWP **(Electrowetting)**	**Liquavista(Samsung)** **ITRI**	**Quick response** **good for color and video applications**	**High driving voltage**
EFD **(Electrofluidic)**	**Gamma Dynamics**	**>85% white-state reflectance good visual brilliance** **Brightness, color situation, video speed**	**High power consumption**
IMOD **(Interferometric MODulation)**	**Qualcomm(Mirasol)**	**Fast refresh speed for video application** **Low power consumption(<E-ink)**	**Small view angle** **Production cost**
ECD **(Electrochromic)**	**Siemens** **Ricoh** **Samsung**	**70% white-state reflectance** **No color filter**	**Color reproduction** **Driving speed**
Ch-LCD **(Cholesteric)**	**Kent Display** **ITRI** **Fujistu**	**Good reflectivity** **Color display without color filters** **Synergy to LCD production**	**Temperature dependence** **Low driving speed poor gray scale**

Table 1-1 Comparison of the main technologies of the electronic paper display

Electronic paper display is currently in a critical phase of its development. Many potential technologies are racing for the future's tremendous market demand. Currently the e-ink technology has achieved the leading position in the monochromatic field due to its good image quality and lower cost. When the electronic paper display comes to the color generation, e-ink's technology loses its superiority because the color filter in the electrophoretic display reduces the reflectivity which will cause the display to be dark. The IMOD display dominated by Qualcomm is good for the low power consumption and higher color reproduction. However, because Qualcomm could not manage to overcome the high production cost. The plan to commercialize this e-paper has been stopped. The Cholesteric LCD is a lower power display due to the bi-stability. The image can be maintained in the display at zero electric field for months. The color display is easy to make in the Ch-LCD by using either three layer stack method or one layer method. It is easy to compatible with the R2R process which will largely reduce the production cost and the scale will be unbounded.

As a summary, which technology would be the strongest contender remains unclear. It would be contingent upon which technology could effectively overcome its deficiencies and could be produced at an acceptable cost. In my opinion, the cholesteric LCD (Ch-LCD) is a promising

technology due to its relative advantage and bright prospect compared with other color e-paper displays. One of the obstacles to its success is lack of effective driving method and fast driving speed for this kind of display which is the scope of this thesis. In the next chapter we will discuss the intrinsic physical and optical characteristics of Ch-LCD.

2. Physical and Optical Characteristics of Cholesteric LCD

2.1 Introduction

Cholesteric liquid crystal display (Ch-LCD) is a special type of liquid crystal display (LCD). The meaning of the term "cholesteric" differs from that in the medical domain. It is made by adding chiral molecules into the nematic liquid crystal to behave as a helical structure, which is similar to the molecule structure of the natural cholesteric. [14] This is also the reason why it was called the chiral nematic liquid crystal. Figure 2-1 shows a picture of the cholesteric LC cell which was taken by optical polarizing microscopy[4].

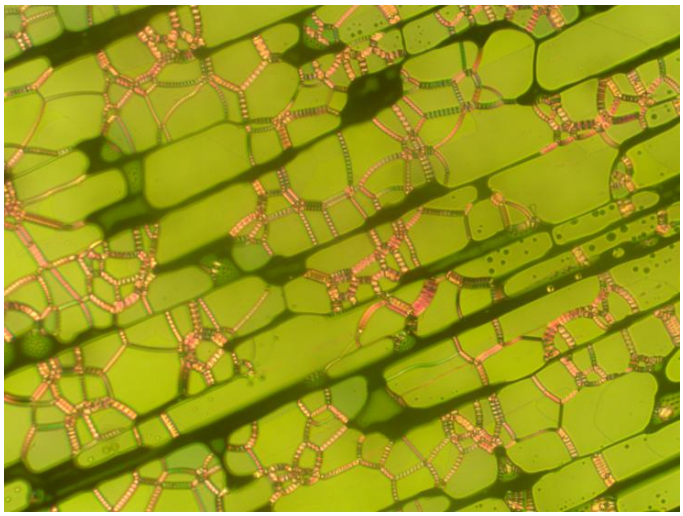


Fig. 2-1 Cholesteric liquid crystal cell picture taken by optical polarizing microscopy

Unlike the conventional LC, the cholesteric liquid crystal molecules form a helical structure, which behaves as two stable states at zero electric or magnetic field. It also has two meta-stable states which could be achieved only by applying a certain voltage level. The planer state of the Ch-LC reflects the light at certain region of wavelength which could be adjusted by adding different dopants leading to different colors' texture. High contrast ratio is also possible through the reflective planer and the scatter focal conic state with a dark backplane. Several meta-stable states could be achieved only if some certain outer conditions are fulfilled, but they are critical in the fast driving schemes. Other characteristics such as the optical properties and the hysteresis are also discussed in this chapter.

[4] Naturally Brilliant Color Inspired By Nature, located on the web page: http://www.qualcomm.com/mirasol/benefits

2.2 Molecule Structure of the Ch-LC

The cholesteric molecules are naturally oriented in the same direction in one layer and the direction is rotated around the helical axis when it is sandwiched in the middle of two substrates. As shown in Figure 2-2, the distance for the direction in one layer to rotate 360 ° is called the pitch of the cholesteric LC. The pitch of the cholesteric liquid crystal could be adjusted by adding different chiral molecules as well as UV radiation, in this way different colors of cholesteric liquid crystal could be achieved. However, the negative point is that the pitch could also be changed by the environment temperature which makes it unendurable to a wide range of temperature shift. In practical applications, the temperature compensation circuit is needed to maintain the stability. [15]

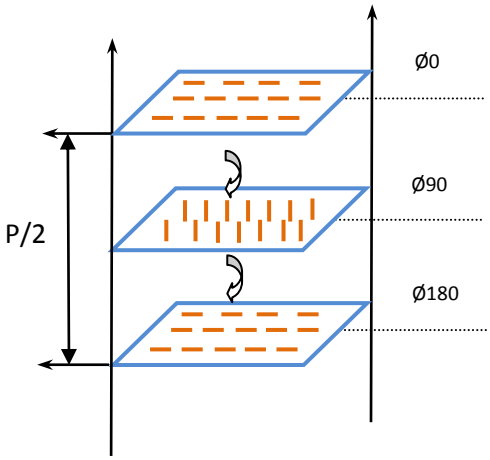


Fig. 2-2 Molecule structure of the cholesteric

The pitch of the cholesteric liquid crystal could be adjusted by varying the concentration of the chiral dopants. The relationship could be expressed by equation:

$$P_0 = \frac{1}{(HTP)x}$$

The HTP denotes the helical twisting power and the x denotes the concentration of the chiral dopants. [16] In addition, the pitch of cholesteric liquid crystal could also be affected by the boundary conditions depending on the display structure and the environmental temperature.

2.3 Stable States of the Ch-LC

As a bi-stable liquid crystal material, the cholesteric liquid crystal has two stable states when it is sandwiched between the two substrates, namely planer state and focal conic state. These two states

could be maintained in the display up to several months without any power consumption. Before 1990 the cholesteric liquid crystal suffered many obstacles such as ultra high driving voltage, small viewing angle etc, as the potential of bi-stability was not fully recognized. After the two stable states of the material had been rediscovered in 1990, the performance of the cholesteric liquid crystal display has been improved continuously. [17]

Figure 2-3 below shows the form of cholesteric liquid crystal when aligned in the brighter planer state. In the planer state, the helix axes of the texture are perpendicular to the cell surface. Thus the incident light is reflected according to the Bragg's law and the display appears white/bright.

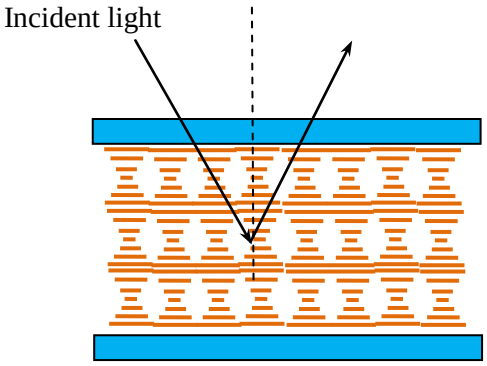


Fig. 2-3 Molecule structure of planer state Ch-LC

When the cholesteric liquid crystal is in the focal conic state, as depicted in Figure 2-4, the helical axes would be randomly orientated and the incident light into the liquid crystal texture would be weakly scattered.

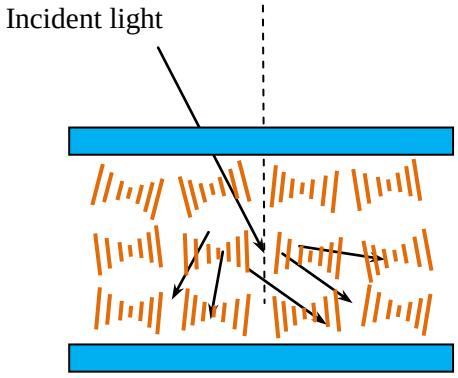


Fig. 2-4 Molecule structure of the focal conic state Ch-LC

So, if the texture is aligned into the planer state, the cholesteric panel would appear bright due to the strong reflectance. On the other side, when the cholesteric texture is aligned into the focal conic state, the display would turn dark because the incident light is scattered. This unique characteristic is perceived as the on and off of a display cell.

Unlike the two stable states which could maintain themselves without any power supply, there also exist other intermediate states which are essential for the driving of the Ch-LCD.

2.4 Meta-stable States of Ch-LC

There are also two meta-stable states which can be achieved under certain voltage field crossing the cholesteric texture, namely homeotropic state and transient planer state. Inside the homeotropic state, the helical structure is broken by the applied voltage field. In this state, all liquid crystal molecules are along with the direction of the electrical field. So the liquid crystal texture becomes transparent. The homeotropic state of the cholesteric liquid crystal is meta-stable state. It could only be maintained when the applied voltage field exceeds a certain threshold value. The cholesteric texture will transform to the homeotropic state if the applied voltage field is stronger than the threshold Ec as described below independent of their initial states. In the equation below, K_{22} is the twist elastic constant, ϵ is the dielectric anisotropy and Po is the pitch of the cholesteric liquid crystal. [18]

$$Ec = 2\pi^2 \sqrt{\frac{K_{22}}{\epsilon}} \frac{1}{Po}$$

Figure 2-5 shows the molecule structure of the homeotropic state of the cholesteric texture. When the voltage field above Ec was applied, the cholesteric liquid crystal's helical structure would be broken and the molecules would in the same direction as that of the applied voltage field as shown in Figure 2-5. In the homeotropic state of the cholesteric LC, the incident light passes through the liquid crystal. Consequently, the cholesteric liquid crystal would become transparent in this state. This transient state cannot be maintained when the voltage field is missing. After removing the applied field, depending on the speed of the removing, the homeotropic state cholesteric liquid crystal would be quickly released to the planer state or to another meta-stable state named transient planer state.

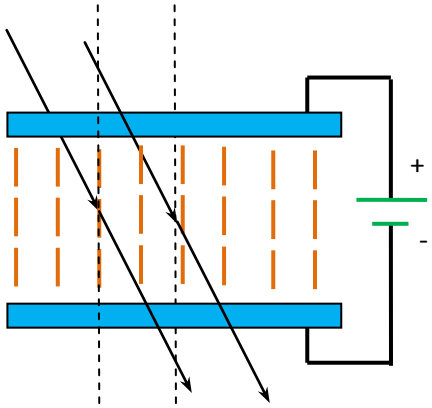


Fig. 2-5 Molecule structure of the homeotropic state of ChLC

The transient planer state is also a meta-stable state. When the cholesteric texture is driven to the homeotropic state by a strong voltage field, the homeotropic state texture would shift to the planer state or the transient planer state depending on the speed of removing the applied voltage field. If the voltage field is removed slowly, the homeotropic state texture will first remain in a transient planer state. Then it will evolve to the focal conic state. In the other case, if the voltage field is removed quickly, the homeotropic state texture will migrate to the planer state. The structure of the transient planer state is depicted in Figure 2-6 below.

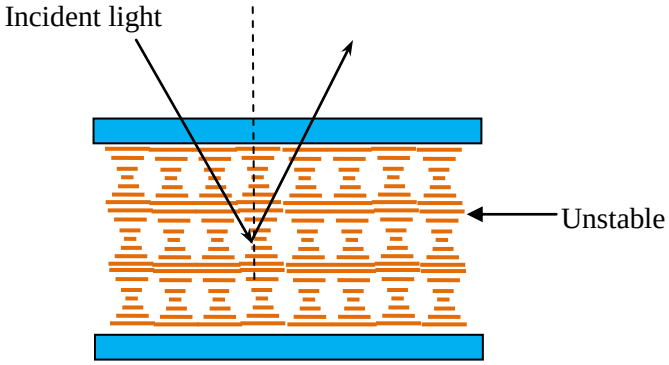


Fig. 2-6 Molecule structure of transient planer state Ch-LC

We can observe that the molecule structure of the transient planer state is almost the same as that in the planer state but not stable. The transient planer state is a critical state which is needed in DDS for the fast driving of the Ch-LCD [19]

The stable and meta-stable states of the Ch-LCD could be used for the fast driving of this kind of display and the bi-stability is achievable thanks to the hysteresis characteristic of the Ch-LC.

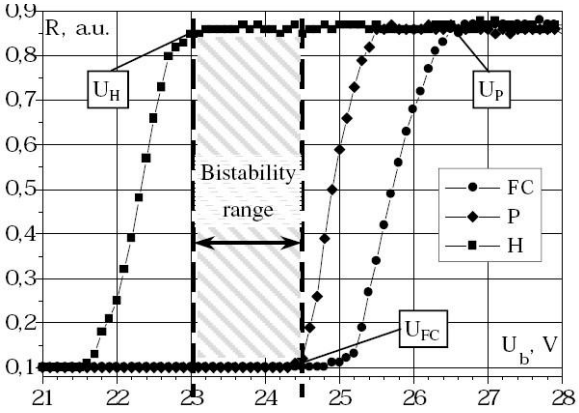


Fig. 2-7 Hysteresis characteristics of the Ch-LC

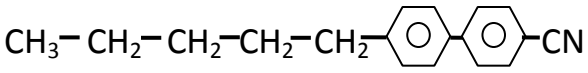
Figure 2-7 shows the hysteresis characteristics of a typical cholesteric liquid crystal material. The x coordinate defines the applied voltage and the y coordinate is the reflectivity. It could be observed from the figure above that the hysteresis between the transition from the planer to the focal conic state and the transition from the focal conic to the planer state is less than two volts. This gap is the bi-stability region. [20]

The unique characteristics of the Ch-LC are caused by the molecule structure which will be discussed below.

2.5 Material and Stability Mechanism

The cholesteric texture used in the display is a mixture of the nematic liquid crystal and chiral dopants.

a. Nematic Liquid Crystal 5CB



b. Chiral Dopant CB15

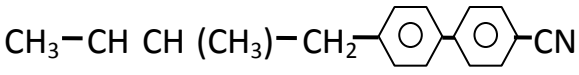


Fig. 2-8 Molecule structure of the typical N-LC and chiral dopant

Figure 2-8 shows the molecule structure of the nematic liquid crystal 5CB and the chiral agent CB15 used for producing the cholesteric liquid crystal material. The molecule structures which are

listed here is the most commonly used material structure for the production of the Ch-LC display. [21]

In the nematic liquid crystal such as cholesteric LC, the stable planer and focal conic state could be achieved by two major mechanisms. The first one is called surface stabilized cholesteric texture (SSCT), and the other one is polymer stabilized cholesteric texture (PSCT) developed by Kent Display. Both of the two methods are aimed to enable the cholesteric texture to achieve the two stable states at the same time. That is to say, the activation energy for both states has to be sufficiently low to form stable states. Each of the two methods is achieved by adding certain materials. Most of the cholesteric LCs are aligned in the PSCT mode. In the normal mode of PSCT cholesteric LCD, the focal conic texture is stabilized at zero electric field. The stabilized focal conic state texture is a poly-domain structure and it could scatter the incident light strongly. Moreover, the texture can be switched to the transparent homeotropic texture through an electric field. [22]

2.6 Optical Properties

The planer state of the cholesteric texture only reflects certain wavelengths of light. When the light is incident to the surface of the planer state texture at an angle θ, only light having the wavelength around λ would be reflected. The critical wavelength could be expressed by the equation below:

$$\lambda = 2\tilde{n}\frac{Po}{2}\cos\theta = \tilde{n}Po\cos\theta$$

Where ñ denotes the average refractive index. θ: the angle of the incident light and Po: the pitch of the cholesteric texture.

The typical reflection spectrum of the cholesteric texture could be illustrated in Figure 2-9. The horizontal axis defines the wavelength of the reflected light and the vertical axis is the ratio of the reflectance.

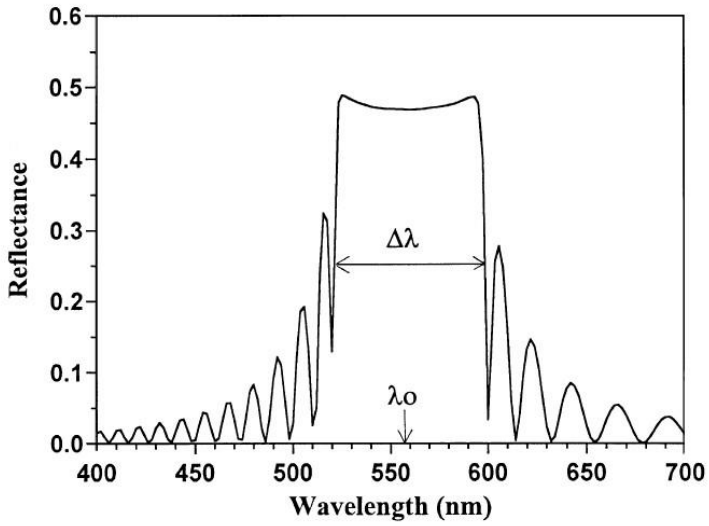


Fig. 2-9 Reflection spectrum of Ch-LC vs. linear polarized incident light on planer state

The $\Delta\lambda$ here denotes the width of the reflection band. The planer state cholesteric texture could reflect about 50% of the un-polarized light. On the other side, the focal conic texture has a very dark optical appearance because the incident light is scattered. [23]

The wavelength of the reflected light can be adjusted by changing the pitch of the cholesteric texture. Normally, the method is to add certain dopant as well as to be irradiated under various ultraviolet processes. In such a way, the wavelength of the reflected light could be precisely controlled in the domain of visible light. Thus, the reflective planer state in the cholesteric LC could display different colors.

This characteristic enables the color cholesteric LCD without usage of color filter that were not possible many other E-paper technologies, giving the cholesteric LCD a natural advantage among the next generation color e-papers.

Figure 2-10 shows the reflection spectrum of the two stable states, the planer and focal conic state. In the cholesteric LCD, usually a black backplane is used to absorb the light which leads to a darker appearance as well as higher contrast ratio.

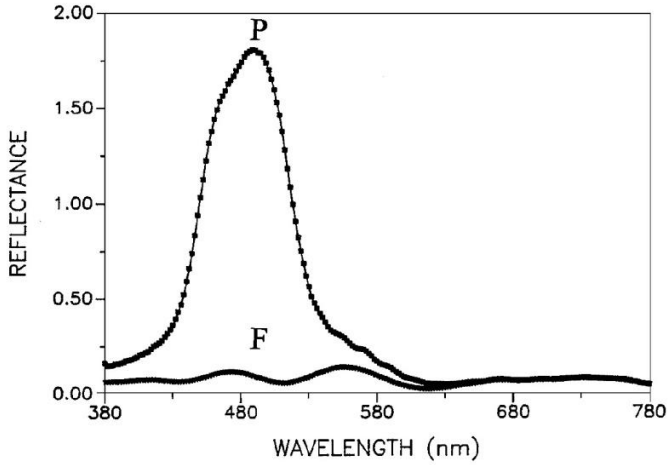


Fig. 2-10 Reflection spectrum of Ch-LC vs. wavelength of the linear polarized incident light on two stable states. (The reflectance unit is arbitrary.)

2.7 Conclusion

In this chapter, the basic physical and electro-optical characteristics of the cholesteric LC are shown. Two meta-stable states namely homeotropic and transient planer state are rediscovered for fast switching between the two stable states. The optical properties and stable mechanism of the cholesteric texture are also discussed. These unique characteristics of the cholesteric LC make it an ideal candidate for electronic paper that could be extended to many applications. However, the color gamut and the color saturation of cholesteric liquid crystal need to be further improved. In the lab level, the color cholesteric LCD by using 3 layers' stack has been made by Fujistu, besides, ITRI also developed the one layer color cholesteric LCD. But both still need to improve the reflectivity and the color reproduction in order to emerge as a leader in the market. We will introduce in the next chapter several driving schemes, and how to effectively drive the Ch-LCD between the two stable states.

3. Driving Schemes of the Cholesteric LCD

3.1 Introduction

It has been several decades gone since the cholesteric liquid crystal was deemed to a promising candidate for electro-optical flat plane display. However, one of the primary obstacles between the thought and realization is the lack of convenient and effective methods to switch between the two stables states which are bright planer state (P) and dark focal conic state (FC) at a high speed. [24] In this chapter, we will discuss the transition mechanism among all of the states the cholesteric LC could have. The development of the driving scheme from the conventional driving method to the fast dynamic driving method will also be introduced in details. As an improvement, an enhanced dynamic driving scheme with gray scale's capability would also be proposed.

3.2 State Transition of the Ch-LCD

As a bi-stable reflective display, unlike the normal liquid crystal display, the cholesteric texture could maintain in its two stable states after removing the applied voltages. Thus the driving of the cholesteric LCD is actually to switch the cholesteric texture between the two stable states.

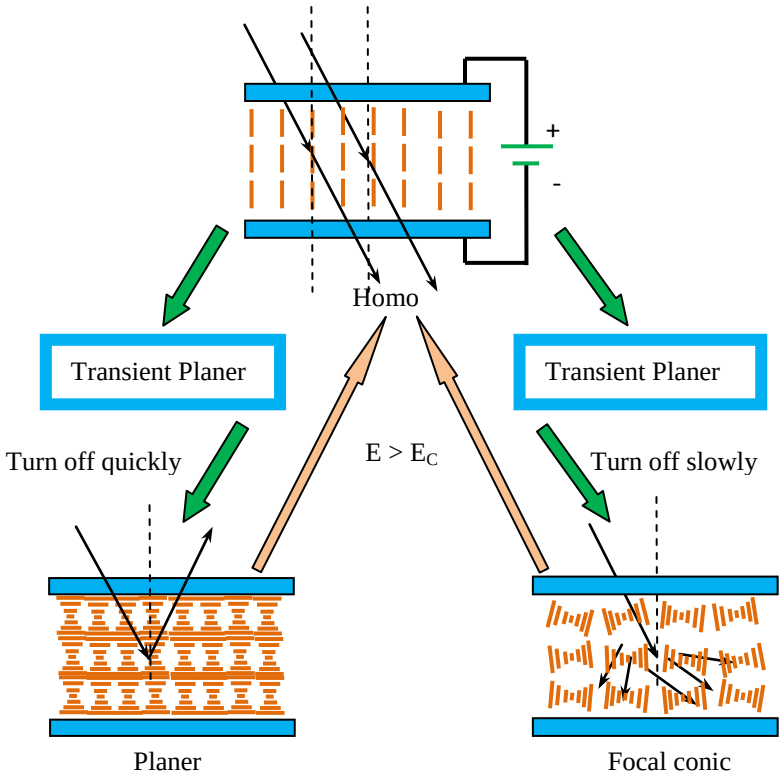


Fig. 3-1The switching sequence among several states of cholesteric LCD

Due to the intrinsic characteristics of the cholesteric texture, the fast switching between the two stable states needs through other meta-stable states. Figure 3-1 illustrates the switch diagram of the several states of the cholesteric liquid crystal display. As we have introduced in the last chapter, planer and focal conic states are two stable states if no additional voltages are applied. In the stable states, the cholesteric molecule will aligned into a helical structure. The difference between the two stable states is that direction of the helical axis.

In the planer state's texture, the helical axis is all aligned into the same direction and perpendicular to the cell surface, thus the incident light would be reflected by the texture and the pixel would be bright. While in the focal conic state, the helical axis is randomly oriented in the texture. Then the incident light will be scattered and the pixel appears dark.

The mechanisms for switching between the two stable states are quite different. If the texture is initially in the planer state, switching from planer to the focal conic state is simple. The electric field across the display cell would make the planer texture instable because the liquid crystal will perpendicular to the field and the electric energy in the cell will be quite high. Thus the liquid crystal would be switched to the focal conic state in which the axis is parallel to the field and the electric energy would be reduced. The achieved focal conic state texture would be stable when the applied field is removed. This process usually needs around 1ms to get completed. However, if we want to switch back to the planer state from the focal conic state, the process would be more complicated. In general, it has to be performed in two steps. In the first step, the focal conic state texture has to be switched to a so called homeotropic state first by applying a voltage which exceeds certain threshold voltage which is thus high enough to make this transition. The value of the threshold voltage could be expressed below:

$$Ec = \frac{\pi^2}{P_0}\sqrt{\frac{K_{22}}{\varepsilon_0 \Delta\varepsilon}} \qquad 3\text{-}1$$

As expressed in equation 3-1, the threshold voltage Ec is related to several parameters. P_0 is the pitch of the cholesteric texture and the K_{22} is the twist elastic constant.

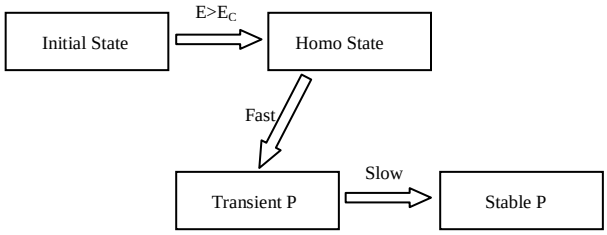


Fig. 3-2 The transition diagram from the initial state to the planer state

Figure 3-2 illustrates the transition diagram of the cholesteric texture switching from the initial state to the planer state. As shown in Figure 3-2, when the applied electric field $E > E_C$, the field

would be high enough to unwind helical structure of the molecules. In this situation, all of the molecules will along with the direction of the electric field and the texture will become transparent. Thus, the cholesteric texture would be held in homeotropic state. If the applied field was turned off quickly, the homo state texture would relax to the planer state in two steps. In the first step, the high voltage maintained homo state texture would be switched to a transient planer state which is not stable. In the second step, the texture would be switched from the transient planer state to the stable planer state. The transient planer texture has a pitch of $2P_0$ [25]. This transition normally needs 10 ms to complete depending on different cholesteric textures and conditions.

3.3 Conventional Driving Scheme

Before the meta-stable transient planer state of the Ch-LC is fully recognized by people, the cholesteric LCD was driven by the conventional way which is to switch between the two stable states directly one row after another. This driving scheme is called static driving scheme comparing to the dynamic driving scheme which will be discussed later. The static driving is to scan pixel by pixel from the top to end of the display and the timing sequence is depicted below.

Figure 3-3 shows the time sequence of the typical static driving scheme. The conventional driving method is quite slow because the next row could be scanned only when the scanning of the last row is finished.

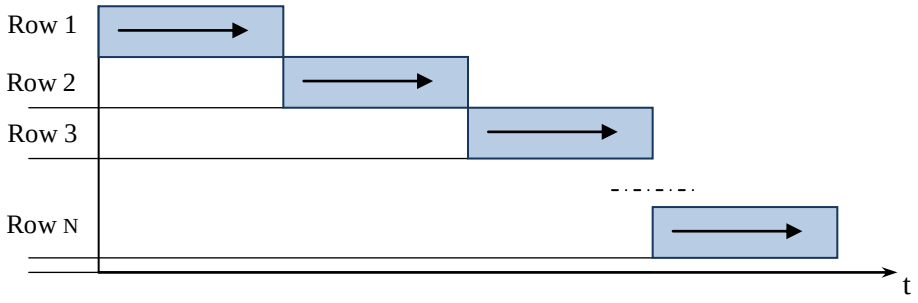


Fig. 3-3 Timing diagram of the static driving scheme of the Ch-LCD

The static driving scheme needs more than 50 ms to refresh one row leading to a low driving speed. This driving scheme allows higher contrast ratio as well as higher image quality because the former created rows will not be affected by the driving waveforms applied to the rows after them. However, the fatal drawback of it is the awfully long driving time. For a 100 rows display, usually 5 seconds will be needed to refresh an image. [26]

In the conventional driving scheme, the waveforms from the related row i and column j are added simultaneously to the aimed pixel P_{ij}. By adding different phases of waveforms from the row and

column lines, the resulted effective voltage field across the pixel will be either in a high or in a low level. By controlling the amount of the effective voltage field applied across the pixel, the controlled pixel could be switched either the planer state or the focal conic state. Figure 3-4 illustrates how the pixel is controlled in the conventional driving scheme.

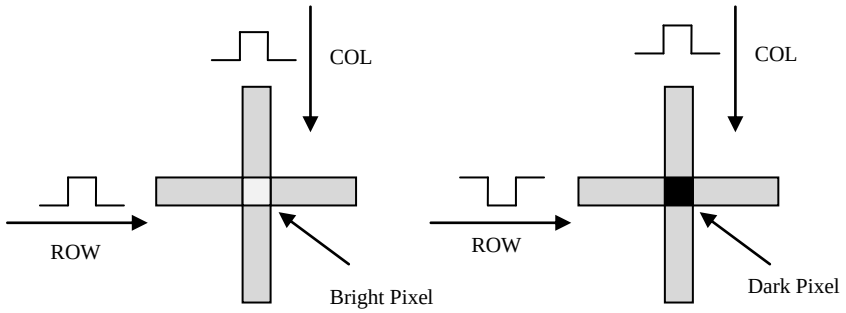


Fig. 3-4 driving method of the conventional driving scheme

The static driving of the cholesteric is simple and easy to achieve high image quality. Besides, because the driving of one row doesn't have any influence on other rows, the crosstalk would not be a problem. The robustness against temperature's fluctuation would also be good for the static driving. However, as we have discussed previously, the awfully long driving time of this driving scheme is an obvious deficiency.

3.4 Dynamic Driving Scheme (DDS)

Along with the resolution of the cholesteric LCD getting higher, the conventional driving scheme costing more or less 50ms per line becomes unpractical. Considering the unique characteristics of the Ch-LC, in 1995, X.Y. Huang etc. suggested a new driving method [27] called dynamic driving scheme which has the ability to drive the cholesteric LCD as fast as 1ms per line in spite of how many lines was controlled. The dynamic driving scheme makes use of the fast transition from the meta-stable homeotropic state to the transient planer state and the hysteresis between the planer state and focal conic state.

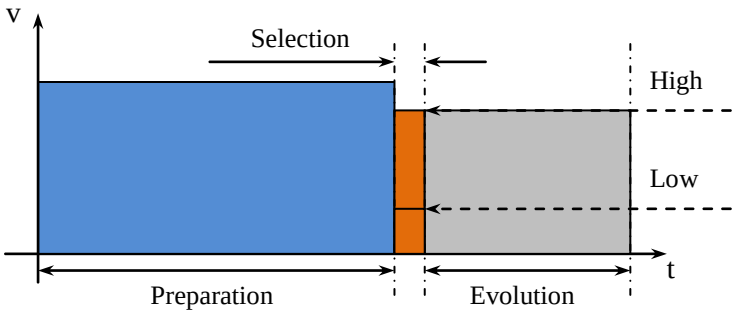


Fig. 3-5 Driving sequence of one row in the dynamic driving scheme

Figure 3-5 shows the driving sequence of the dynamic driving scheme proposed by X.Y. Huang etc. Different from the conventional driving scheme, all pixels are firstly switched to a meta-stable homeotropic state. After that pixels are switched from the homeotropic state to a transient planer state in a quite high speed. This characteristic was introduced to drive the cholesteric LCD with a short driving time in the range of 1 millisecond.

Huang etc. suggested a three stages driving sequence in the dynamic driving scheme as shown in Fig 3-5. The three stages were called preparation stage, selection stage and evolution stage. Driving waveform used in this scheme is a 1000 Hz alternating pulse wave.

To better explain the dynamic driving scheme, we would like to introduce the R-V curve of the cholesteric LCD. Figure 3-6 shows reflectance versus applied voltage of the cholesteric texture. As marked in the image by a yellow arrow, the homeotropic state will be fast switched to a transient planer state by applying a low voltage in the selection stage. Then the selected texture will slowly evolve to the focal conic state. The evolving time could be overlapped during adjacent lines, thus the driving time increases with the number of rows only in the selection stage.

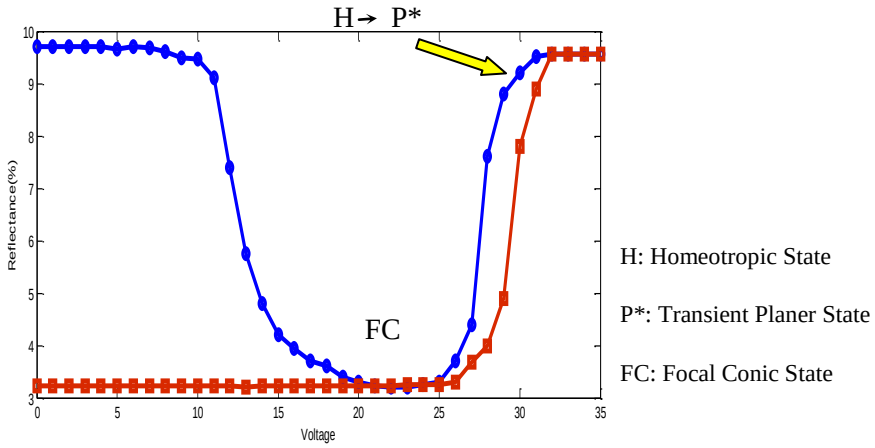


Fig. 3-6 Reflectance vs. Voltages in the Cholesteric LCD

First of all, in the preparation stage, higher driving voltage was added and sustained for 60 ms to refresh all pixels into the homeotropic state. After that, in the selection stage, driving waveform would determine that the selected pixels were switched to the planer state or eventually transferred to the focal conic state.

The selection was executed by controlling the effective electric field in the selection stage. If a higher electric field is added, the homeotropic state texture will be kept, on the contrary, if the added electric field was low enough, the homeotropic texture in the selection stage will be changed to the transit planer state.

The third stage was named evolution stage. This stage combined with the selection stage was designed to complete the process of the transition. In the selection stage, if the pixel was kept in the homeotropic state, the electric field in the evolution state will keep maintaining it at that state until the end of the driving waveform.

In the end of the driving sequence, when the evolution's electric field was turned off, the maintained homo state pixels will quickly be switched to the planer state. On the other side, if the pixel was given a low electric field in the selection stage, the achieved transit planer pixels will change to the focal conic state slowly during the process of the evolution state. After the evolution stage was turned off, stable focal conic state pixels will be achieved. [28]

Figure 3-7 below illustrates the schematic diagram of this dynamic driving scheme. We could compare it with that of the conventional driving scheme. The specific difference is, in the dynamic driving scheme, when the first row is still in progress, the next several rows will already start to be processed.

In the dynamic driving scheme, the preparation and evolution stages are still kept in their original lengths. However, because the preparation and evolution waveforms are overlapped among lines in time, the total driving time of the whole scheme for a N rows display would be as long as the time needed for one row in the two stages (Preparation and Evolution stages) plus the N×Ts(selection time). Considering a 1000-line Ch-LCD, only 1080 ms equals 1.08 s was needed which is much more reasonable than the conventional driving scheme. [29]

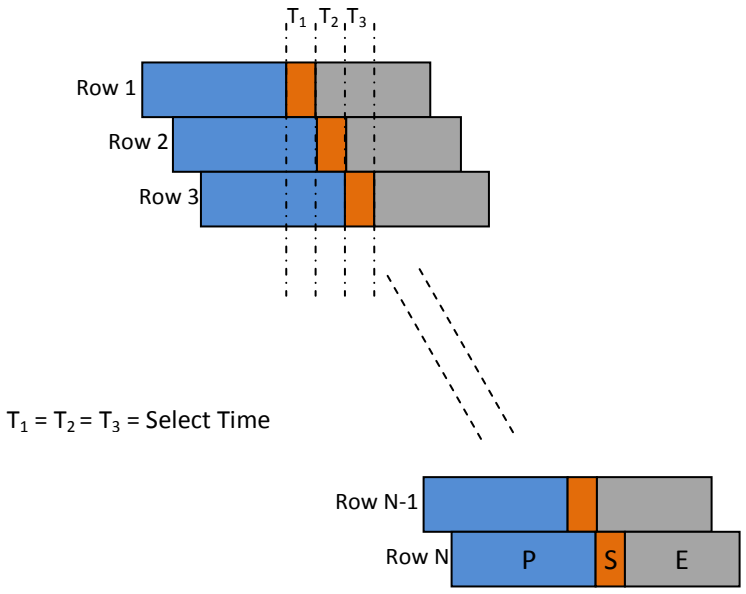


Fig. 3-7 Schematic diagram showing how the Ch-LCD is addressed in DDS

As the first try, the dynamic driving scheme proposed in 1995 has largely increased the driving speed of the cholesteric LCD. However, it still has a lot of room to improve. Firstly, the number of voltages for the driving scheme is still quite high. A common solution with four voltages in rows and two voltages in columns will increase the driver chip's complexity. Secondly, voltages used in the dynamic driving scheme are in really high values leading to high power consumption. As an improvement, a dynamic driving scheme named U/$\sqrt{2}$ was proposed by A. Kozachenko in 1997. [30]

3.4.1 DDS U/$\sqrt{2}$

The U/$\sqrt{2}$ dynamic driving scheme (DDS) features a quite simplistic waveform pattern and only two voltages are needed for the whole driving scheme, which are U and zero. The cross pixel's electric field have three possibilities, U, -U and zero.

Figure 3-8 shows the waveform pattern of the U/$\sqrt{2}$ dynamic driving scheme on a 3×2 pixel matrix. The waveform part marked by orange color is the waveform in the selection stage of the driving scheme.

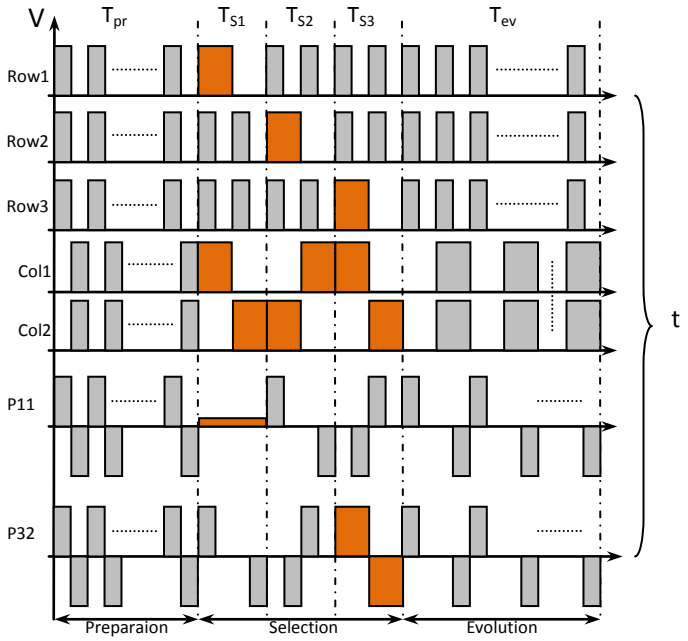


Fig. 3-8 Sample of the U/$\sqrt{2}$ DDS for a 3×2 Ch-LCD pixel matrix

Different from the first dynamic driving scheme, in the U/$\sqrt{2}$ dynamic driving scheme, the whole driving scheme was divided into four stages, which are preparation stage, selection stage, holding stage and evolution stage. The holding stage is placed before and/or after the selection stage to hold the cholesteric texture. The arrangement of the four stages could be observed in Figure 3-9.

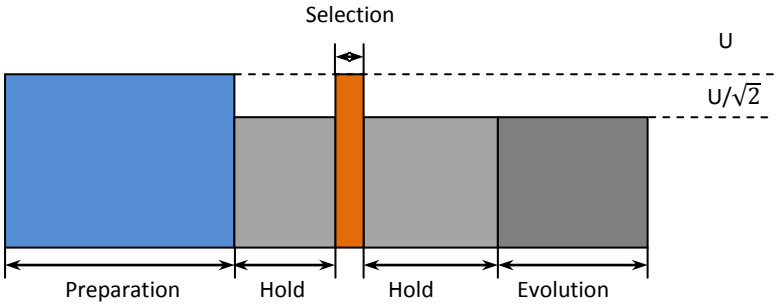


Fig. 3-9 Driving stages of the U/$\sqrt{2}$ dynamic driving scheme

The critical voltage U is used in the preparation stage to refresh all pixels of the display into the homeotropic state. The holding stage is between both of the preparation and selection stages and/or selection and evolution stages. The holding part before the selection stage is to hold the homeotropic state until the selection stage comes. Holding part after the selection stage is to combine with evolution stage to let the selected pixels evolving to the focal conic state. The RMS voltage U_H in the holding stage and the RMS voltage U_E in the evolution stage have the constant ratio with the preparation voltage U. In these two stages, the voltage is applied for half of the selection time, thus the RMS voltage in holding and evolution stage is $U_H=U_E=U/\sqrt{2}$. The RMS

voltage in the selection stage either in U or zero could select the pixel into the planer or focal conic state.

The U/$\sqrt{2}$ features less number of voltages needed in the whole driving scheme. However, because the effective electric field only exists in half of the holding stages, higher driving voltages are required for achieving a high RMS electric field. In order to reduce the driving voltages in an effective way, another more effectual improvement called U/$\sqrt{\frac{3}{2}}$ dynamic driving scheme would be discussed below. [31]

3.4.2 DDS U/$\sqrt{\frac{3}{2}}$

As it was named, the U/$\sqrt{\frac{3}{2}}$ dynamic driving scheme also has constant correlations among the effective voltage values of the four driving stages. Different from the U/$\sqrt{2}$ scheme, the number of subdivision is six in all of the stages excluding the preparation stage. As to the waveform type, the root of mean square value of effective voltage could be higher than that in the U/$\sqrt{2}$ under the same applied voltage U. Thus, the applied voltage could actually be reduced by 18% in this scheme. The timing diagram of the U/$\sqrt{\frac{3}{2}}$ dynamic driving scheme is depicted in Figure 3-10.

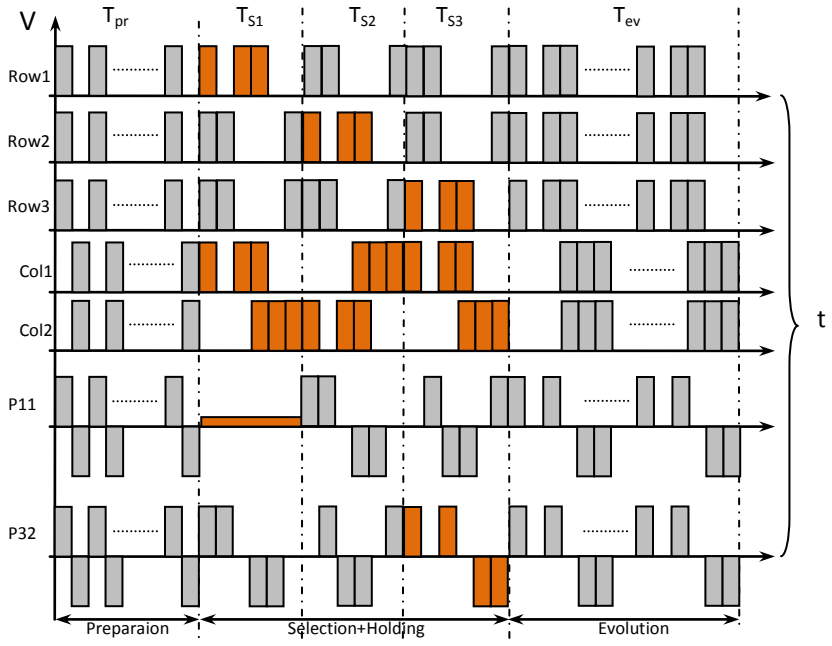


Fig. 3-10 Sample of the U/$\sqrt{\frac{3}{2}}$ DDS for a 3×2 Ch-LCD pixel matrix

As to the timing diagram, a sample of 3×2 pixel matrix was selected. From the timing diagram of the U/$\sqrt{\frac{3}{2}}$ dynamic driving scheme we could observe that in selection, holding and evolution stages, if the pixel was planned to selected to planer state, the cross pixel's voltage is for 2/3 of the driving time high. On the contrary, if the pixel was planned to selected to the focal conic state, the cross pixel's voltage will be zero. The effective voltage field added on the pixel could be calculated according to the equation below:

$$V_{rms} = \sqrt{\frac{V_1{}^2T_1 + V_2{}^2T_2 + \cdots V_n{}^2T_n}{T_s}}$$

$$= U\sqrt{\frac{T_1 + T_2 + \cdots T_n}{T_s}} \qquad 3\text{-}2$$

T_1, $T_2 \ldots$ T_n are time periods of each pulse $_{\text{when } U \neq 0}$.

As it could be found in Equation 3-2, Ts is the selection time while T_1 to Tn are the time of the sub divisions within one selection stage when the applied voltage is not zero. V1 to Vn are the relevant voltage levels.

Because the cholesteric liquid crystal texture responses to the root of mean square (RMS) of the applied voltages, the RMS voltage value in the selection stage of this driving scheme could be calculated from equation 3-2 that:

$$Vs = U_1/\sqrt{\frac{4}{6}} = U_1/\sqrt{\frac{2}{3}} \qquad 3\text{-}3$$

RMS voltage Vs calculated from Equation 3-3 is for switching the pixel to the planer state or

$$Vs=0 \qquad 3\text{-}4$$

The Vs value in Equation 3-4 is the voltage to switch the pixel into the focal conic state.

On the other side, the RMS voltage value in the selection stage of the U/$\sqrt{2}$ dynamic driving scheme is:

$$Vs=U/\sqrt{2} \qquad 3\text{-}5$$

Vs here in Equation 3-5 is the value which is needed to switch the pixel into the planer state in U/$\sqrt{2}$ DDS or

$$Vs=0 \qquad 3\text{-}6$$

The Vs in Equation 3-6 is the value to select the pixel into the focal conic state in U/$\sqrt{2}$ DDS.

According to the equations above that the cholesteric texture response to the RMS value of the applied voltage, giving the same RMS voltage value in the selection stage. There exists:

$$U_1/\sqrt{\frac{2}{3}} = U \qquad 3\text{-}7$$

Thus, we could conclude that:

$$U_1 = U \times \sqrt{\frac{2}{3}} \approx 0.82\ U \qquad 3\text{-}8$$

$$U_1 / U \approx 0.82 \qquad 3\text{-}9$$

From the computed result in 3-9 we could draw the conclusion that the voltage applied in the selection, holding and evolution stages of the U/$\sqrt{\frac{3}{2}}$ dynamic driving scheme could be 18% less than that in the U/$\sqrt{2}$ driving scheme.

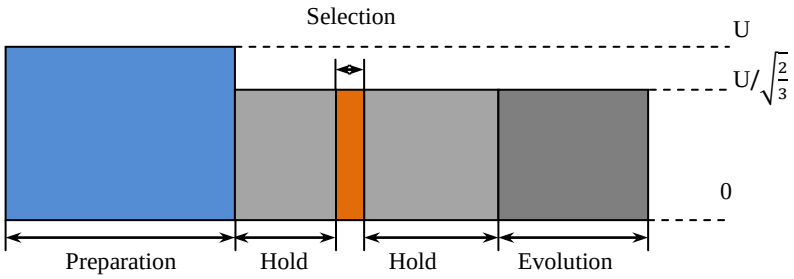


Fig. 3-11 Driving sequence of the U/$\sqrt{\frac{3}{2}}$ DDS

The driving sequence of the U/$\sqrt{\frac{3}{2}}$ dynamic driving scheme includes four stages as could be observed in Figure 3-11, which is almost the same as those in the U/$\sqrt{2}$ DDS. The effective voltage levels in the selection, holding and evolution stages all have the same correlation with the applied voltage U:

$$U_{HOLD}=U_{SEL}=U_{EVL}=U/\sqrt{\frac{3}{2}} \qquad 3\text{-}10$$

That's why this driving scheme was called U/$\sqrt{\frac{3}{2}}$ dynamic driving scheme.

As we have calculated, the six divisions' pattern in the selection stage as shown in Figure 3-10 is more effective to make use of the applied voltage for achieving a higher RMS voltage level. Thus,

the applied voltage could be reduced comparing to that in the four divisions' driving scheme. The eight or more divisions also could be used but the effective RMS values could not get higher. Therefore the six divisions' method of the selection time is reasonable.

It has to be mentioned here that the preparation time of the U/$\sqrt{\frac{3}{2}}$ DDS must be longer than that of the U/$\sqrt{2}$ DDS because the preparation voltage was also reduced.

3.4.3 Fast Dynamic Driving Scheme

In the pursuit of higher driver speed, an effective and reasonable solution is to reduce the selection time as short as possible. A typical approach was proposed for this by A. Rybalochka etc. in 2000. The driving scheme was named fast dynamic driving scheme which has the ability to reduce the selection time 4 to 5 times comparing to the selection time in the normal DDS, usually 1~2 millisecond. [32]

The driving sequence of the fast driving scheme is as follows:

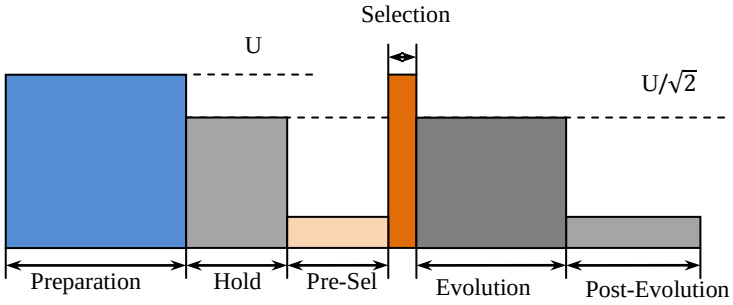


Fig. 3-12 Driving sequence of fast driving DDS

As the driving sequence of the fast driving scheme shown in Figure 3-12, the driving scheme has six driving stage which are preparation, holding pre-selection, selection, evolution and post-evolution stages. Comparing to the U/$\sqrt{\frac{3}{2}}$ DDS, the fast DDS has two more driving stages which are named pre-selection and post-evolution stages.

During the pre-selection stage, the $U_{pre\text{-}s}$ = U_{col} is added to pixels. The voltage U_{col} in the pre-selection stage is set to be low enough to initiate the transition from the homeotropic state to the transient planer state. The voltage field in the selection stage will determine either the pixel will stay in the transient planer state or backing to the homeotropic state.

After the evolution stage, there is also a so called post-evolution stage with the voltage value $U_{p\text{-}ev}$ = U_{col}. The post-evolution stage is not for driving but for the driving principles.

By adopting this driving method, driving speed could be enhanced to 1/4 ~1/5 Γ, the Γ here is the transition time from the homeotropic state to the transient planer state of the cholesteric texture.

Along with the increasing number of the driving stages as well as complexity, the driving speed could be enhanced. However, driving voltages in these methods above are still quite high. On the other side, these DDS only concentrate on the on-off control of the cholesteric LCD but not on gray scales. Thus, DDS with gray scales' capability will be of great interesting.

3.5 Enhanced DDS with Gray Scale Capability

In Euro Display 2011, we proposed an enhanced dynamic driving scheme with the gray scale capability. [33] In the enhanced DDS, six divisions' waveform pattern was used in the selecting and holding stages to reduce the maximum driving voltages. The new DDS with modified preparation and selection waveforms can be easily used to drive the Ch-LCD into both the on-off state and gray scale state. The driving voltages used in this driving scheme are lower comparing to the several ones above. In addition, the number of driving stages and number of voltages needed are both smaller.

This driving scheme includes four main stages which are named preparation stage, holding stage, selection stage and evolution stage. The preparation stage drives all the pixels into homeotropic state. It is followed by the selection stage, which decides whether the pixel is maintained in the homeotropic state or evolving to the transit planar state. If the homo state is maintained, the pixel will be switched to the bright planar state after the evolution stage. On the contrary, if it is transferred to the transit planar state, the pixel will evolve to the dark focal conic state after the evolution stage. There are only three voltage levels used in the whole scheme, namely the higher voltage U_H, the lower voltage U_L and ground. The voltage U_H is used only in the row driving waveforms during the preparation stage to drive all pixels out of their initial state into the homeotropic state.

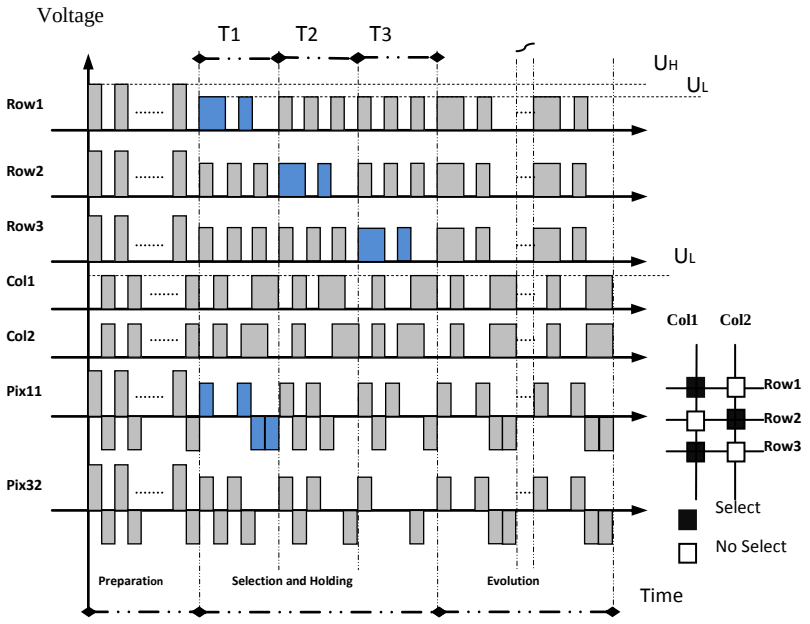


Fig. 3-13 Timing diagram of the enhanced dynamic driving scheme

Figure 3-13 shows the timing diagram and driving pattern of the enhanced dynamic driving scheme in a 3×2 pixel matrix. The preparation voltage used in the row driver is the higher voltage U_H, while in the column driver the lower voltage U_L is used. Therefore, the voltage across pixel is switched between the high and low levels. This driving method consumes less power than the traditional $U/\sqrt{2}$ driving method and we also found out that this waveform pattern produces more stable and reproducible gray levels as will be described in the next chapter.

In contrast to the conventional $U/\sqrt{2}$ driving scheme, in the new selection stage the driving time is divided into six sub divisions instead of four sub divisions. This waveform pattern allows lowering the selection voltage because using the same V_L. The RMS value of the applied voltage level during the holding stage is bigger than that of the $U/\sqrt{2}$ method. The waveform of the new selection stage has also been modified to easily drive the display into gray scale states.

To find the optimal values for the critical parameters of this enhanced dynamic driving scheme, we first applied a waveform with a pulse length of 100 ms to drive one pixel in the demonstration panel from AEG MIS. We found that a voltage of 48V is needed to safely drive the pixel into homeotropic state from any possible initial state.

Preparation Time (msec)	Preparation Voltage (Volt)
24	>60
26.4	57
28.8	56
32.2	55
33.6	53.5
36	53
39	52.5
42	52.5
43.2	52
45	51
48	48
50	48
56	48

Table 3-1 Test of the preparation voltage versus preparation time

The test waveform was then varied from 10 ms to 60 ms, which showed that a preparation stage of 48 ms is sufficient. The transition from the homeotropic state to the transit planar state usually takes in the order of milliseconds to complete. We found that selection times from 1.0 ms to 1.6 ms can be used in the driving scheme at room temperature. By testing, T_s=1.2 ms achieved the best trade-off between contrast ratio and low selection voltage.

Finally, the DDS was operated with fixed preparation and selection voltages and a preparation time of more than 50 ms. The duration of the evolution stage was varied from 2.4 ms to 16.8 ms, showing that at least 16 ms was needed to ensure that the last row is properly driven. The driving waveforms in the evolution phase had the same pattern as the selected waveforms in the selection phase, leaving the RMS value unchanged to get stable gray scale states and to avoid crosstalk. The optimized length of each stage is listed in the table below:

	Driving Stage	Driving Time
1	Preparation Stage	48 ms
2	Selection Stage	1.2 ms
3	Holding Stage	1.2 ms
4	Evolution Stage	16 ms

Table 3-2 Length of each stage in the dynamic driving scheme

As to the waveform pattern, we have to design the driving waveform according to several rules. Firstly, the driving waveform in the selection and holding stages should use the 6 sub division's pattern to reduce the applied voltage for the reason we have discussed before. Secondly, the overlapped driving waveform in the selection stage should be able to drive the cholesteric texture into the planer or focal conic state. Thirdly, the overlapped holding waveform must has the constant duty cycle in order not to affect the selection stage due to the different length of the holding stage in different rows. Besides, the driving waveform should have the gray scale's capability. By complying with these rules, the designed waveform pattern in the selection stage is as follows:

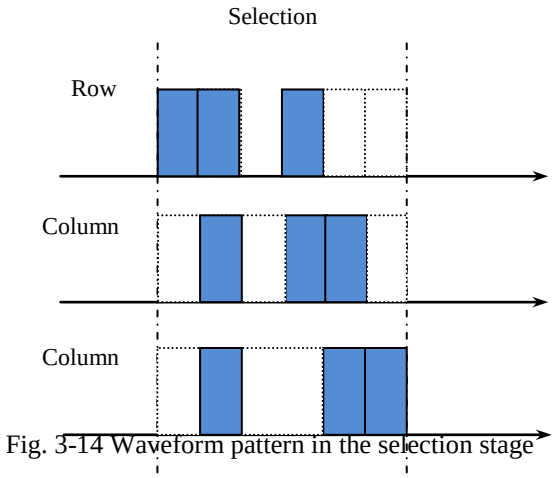


Fig. 3-14 Waveform pattern in the selection stage

As can be observed in Figure 3-14, the waveform pattern in the selection stage includes six sub-parts in both of the row and column lines. The selection waveform in the row and column all take 3 of the 6 sub-parts. Waveform pattern in all the rows are the same. However, waveforms in the column lines have two different arrangements. The upper column waveform is to no-select the pixel and the lower column waveform is to select the pixel.

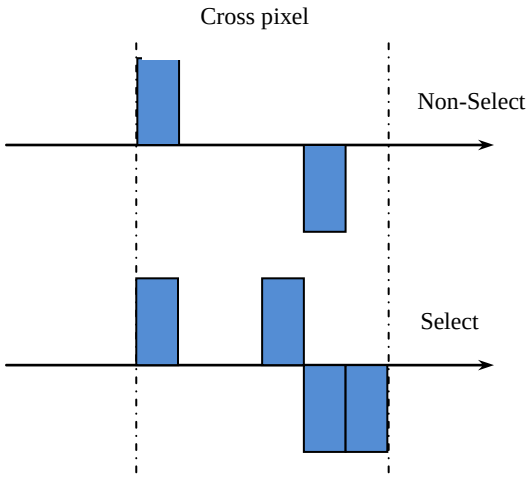


Fig. 3-15 Cross pixel's waveform pattern in the selection stage

Figure 3-15 shows the overlapped cross pixel's waveform pattern. We can see that when the waveform in the column lines is the no-select one, the overlapped waveform is 2 of the 6 sub-parts. And in the select waveform pattern, the overlapped waveform is 4 of 6 sub-parts.

By calculating the RMS voltage values using the equation below:

$$V_{rms} = \sqrt{\frac{V_1{}^2T_1 + V_2{}^2T_2 + \cdots V_n{}^2T_n}{T_s}}$$

$$= U\sqrt{\frac{T_1 + T_2 + \cdots T_n}{T_s}}$$

$T_1, T_2 \ldots T_n$ are time period of each pulse $_{\text{when } U \neq 0}$. 3-11

We can calculate the RMS value that:

$U_S = 0.82U$ and

$U_{NS} = 0.57U$ 3-12

The U in Equation 3-12 is the applied voltage in the selection state. From the calculation above we know that values of Us and U_{NS} are enough to drive the cholesteric texture into either the planer state or focal conic state.

The waveform pattern of the holding stage of the enhanced dynamic driving scheme is also important. In this new dynamic driving scheme, the length of the holding stage before or after the

selection stage will be varied in different rows. Therefore the waveform of the holding stage must match the waveform in other holding stage as well as the selection stage to insure a constant value.

Figure 3-15 shows the designed waveform pattern in the holding stage as depicted below:

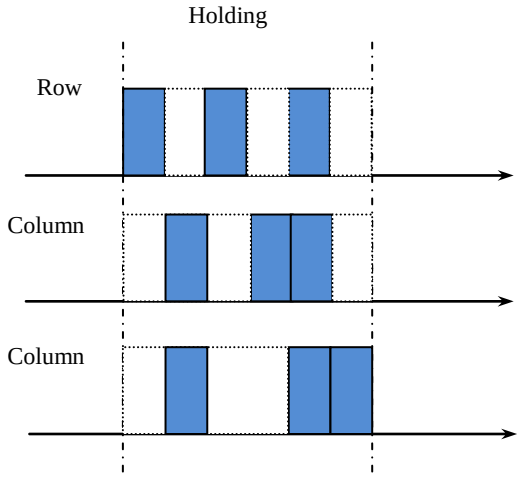


Fig. 3-16 The waveform pattern of the holding stage

Figure 3-16 shows the row and column's waveform pattern in the holding stage. The holding waveform in the row of the cholesteric LCD has the pattern of 3 out of 6 sub-parts as depicted in Figure 3-16. In the column lines, the waveform could only have these two patterns in the holding stage.

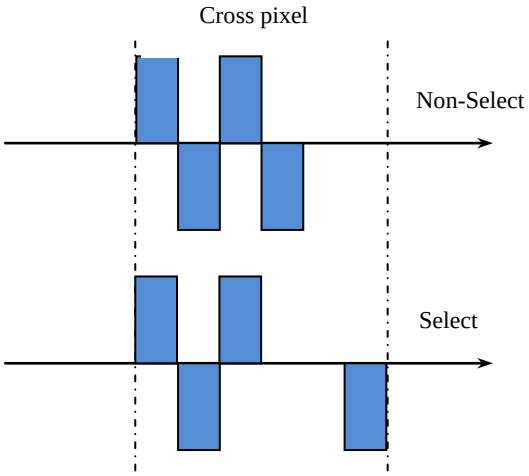


Fig. 3-17 The waveform pattern in the holding stage

From overlapped waveform in Figure 3-17 we could observe no matter it select or no-select, the overlapped cross pixel's holding waveform always has the same duty cycle which is 4 out of 6 sub-divisions. From the equation before we can calculate the value is that:

$$U_H = 0.82\ U$$

This value is the same as the RMS voltage value in the selection stage when selecting. So the pixels have not been selected will be held to the homeotropic state until the selection stage ends or the evolution stage starts.

The waveforms of the preparation and evolution stage are in the typical form of the U/$\sqrt{\frac{3}{2}}$ dynamic driving scheme which do not need to change.

The waveform in the evolution actually has the same function as the part of the holding stage after the selection stage, so the waveform is just needed to keep the same RMS voltage value as that in the holding stage.

The waveform also has the ability to generate the gray scales by moving the column waveform in a certain region which will be described in the next chapter.

The driving sequence of the enhanced dynamic driving scheme is shown in Figure 3-18.

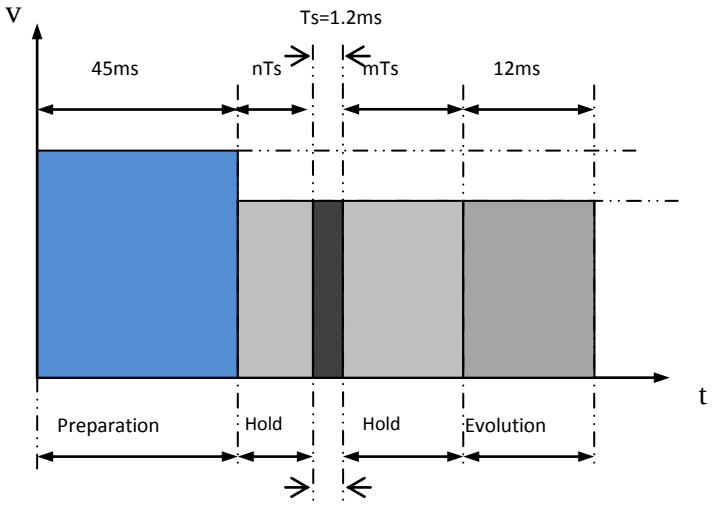


Fig. 3-18 Main driving time used in the DDS

Figure 3-18 shows the critical timing parameters used in the proposed enhanced dynamic driving scheme. These parameters are used in on, off and gray scales' driving for a different number of rows.

Comparing with other dynamic driving schemes we have shown above, the enhanced DDS has the ability to drive the cholesteric LCD into not only the on-off state but also several gray scales by designing new waveform patterns in the selection and holding stages. Different from the five voltages used in the U/$\sqrt{\frac{3}{2}}$ DDS, voltage number in the enhanced DDS was also reduced to only three which are U_H, U_L and zero. Driving speed of 1.2 ms per line in the enhanced DDS is

achieved which is faster than many other DDS. If the U/$\sqrt{2}$ DDS is taken into account, the highest driving voltage was also reduced by 12%.

However, we also found that in driving of the large scale cholesteric LCD，the needed driving voltages will shift a little bit when the number of controlled rows is different.

Figure 3-18 shows the required selection voltage versus the number of rows in the display. We could observe that the voltage has to be increased when more rows are driven. This may be caused by parasitic capacitors between pixels being charged by the applied voltage, consuming driving energy. The increased selection voltage ensures the uniformity of the selected region in spite of the increased power consumption.

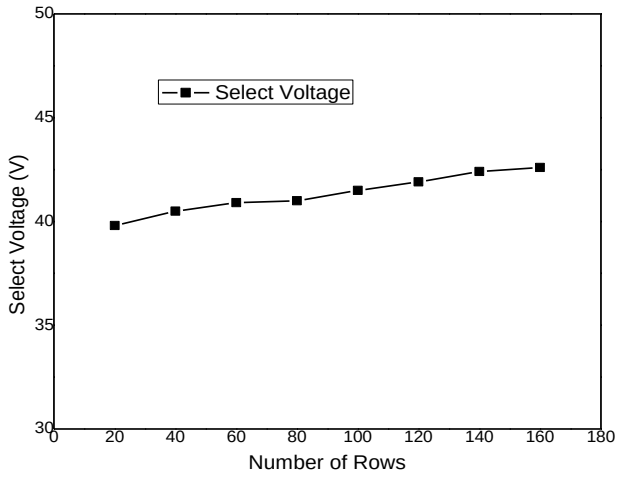


Fig. 3-19 The shift of VL vs. number of controlled rows

To extend this dynamic driving scheme to the 160×160 Cholesteric LCD panel, the highest driving voltage of 42V is needed as can be observed from Figure 3-19.

In order to verify this new dynamic driving scheme as well as the newly designed driving waveform. We have executed it on a cholesteric LCD with 160 lines provides by AEGMIS.

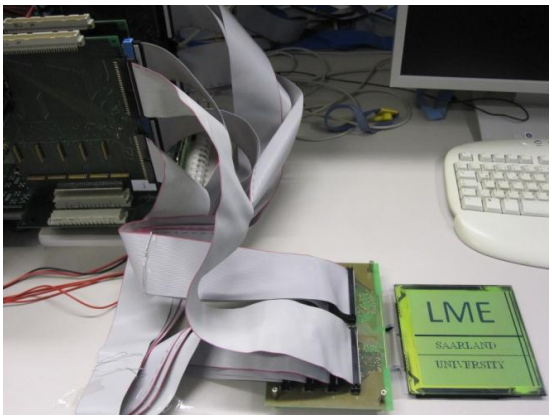


Fig. 3-20 160 rows choesteric LCD is driven by the proposed DDS

As shown in Figure 3-20, test image has been successfully created by adopting the new enhanced dynamic driving scheme on a 160×160 Ch-LCD panels. A Xilinx Virtex-5 FPGA was chosen to control this set. The experimental driver board was constructed using commercially available components and can be easily adapted to test different driving schemes. Details of the design schematic view and related parameters of the discrete driver board could be found in chapter 7.

The dynamic driving scheme realized on this driver board has shown very good contrast ratio and driving speed. The contrast ratio and image quality have no observable reduction than that is created by the conventional driving scheme. The driving speed is about 1.2ms per row with only three driving voltages in all phases. Gray scale could also be created using the same driving scheme which will be described in the next chapter. The generated gray scale values are stable and reproducible.

3.6 Conclusion

In this chapter we have discussed the basic driving principles and switching conditions of the cholesteric LCD. The slow conventional driving scheme and several fast dynamic driving schemes are also elaborated. By considering the deficiencies of the current dynamic driving schemes, we have proposed an enhanced dynamic driving scheme with specially designed waveform pattern for lower driving voltages. The driving scheme also has the ability to drive not only binary-valued image but several gray scales by using the one and the same waveform pattern and voltage groups which, to our best knowledge, has not been mentioned in other dynamic driving schemes. Critical parameters of the driving scheme have been calculated and determined. The method for testing and measuring these parameters are also mentioned. The new dynamic driving scheme has been

executed by the FPGA controller on our test Ch-LCD panel. Reasonable results have been achieved and some unwanted phenomena such as the shift of the driving voltages are described.

4. Gray Scale Driving in Ch-LCD

4.1 Introduction

For the monochromatic application of the single color cholesteric LCD, how to efficiently and economically create the distinct gray scale is always a challenging issue. The static dithering method would drastically reduce the image resolution while the dynamic dithering method is not reasonable for an e-paper, as it would inevitably lead to high power consumption.

As mentioned in the second chapter, the cholesteric liquid crystal has two stable states at zero electric field, called planer state and focal conic state. Inside a pixel of the Ch-LCD, depending on the effective voltage values across the pixel, part of cholesteric texture could be switched to the planer state while others could evolve to the focal conic state. The planar state and the focal conic state can be maintained simultaneously in one and the same pixel of the cholesteric LCD. Such a mixed state is as stable as pure planar or focal conic state. [34] Therefore, by precisely controlling the effective voltage values across a pixel, domain size of the planer texture or focal conic texture could be adjusted. When the proportions of the two states change, the reflectivity of the pixel will be varied, so that different gray scales would be created. Figure 4-1 below illustrates the principle about how the two stable textures may exist in the pixel.

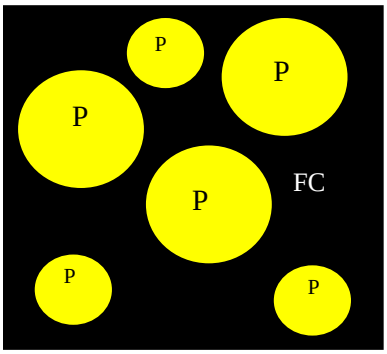


Fig. 4-1 A sketch of the gray scale in a Ch-LCD pixel

Figure 4-1 illustrates how the two stable states could be maintained in the same pixel for generating the gray scale. From chapter 3 we knew that in the dynamic driving of the Ch-LCD, the cholesteric texture switching from the homeotropic state to the focal conic state or planer state is correlated with the voltage field in the selection and holding stages. If the value of effective voltage field in the selection stage varied in a certain region, the proportions of the focal conic state and planer state texture could be adjusted.

Although the generation of the gray scale in the Ch-LCD is theoretically possible, the implementation in the circuit and driving scheme's side is still challenging.

Since the gray scale is related to the voltage field, the simplest solution to achieve the gray scales it to vary the applied voltage in the selection region. It has been realized before, called Pulse Height Modulation method.

4.2 Gray Scale Driving Methods

4.2.1 Pulse Height Modulation

Similar to the method which was adopted in the LCD's driving, one of the driving schemes named PHM (Pulse Height Modulation) has the ability to create gray scales in the Ch-LCD. [35] The PHM method needs to change the applied voltage field very often during the selection time, which would require numerous voltage levels leading to a quite complicated driving circuit.

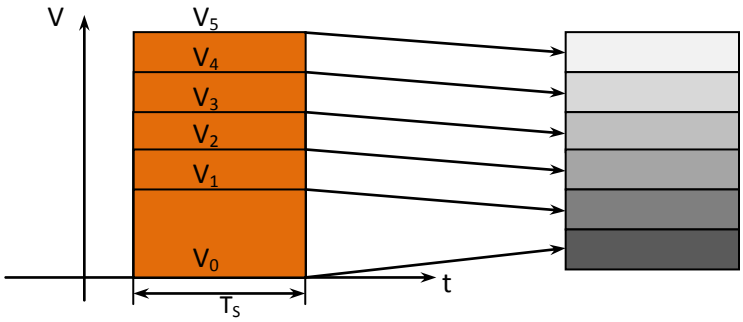


Fig. 4-2 Sketch diagram of the PHM method for gray scale's generation

The Figure 4-2 above shows a sketch diagram of the PHM method which is one of the methods for generating gray scales in the cholesteric LCD. The rationale of this method is to control the effective electric field by switching the applied voltage levels. Voltages in the selection part were generated by an outer driving circuit. When the voltage levels varied between the threshold voltage levels for pure planer and pure focal conic state, the domain size of the planer texture of the pixel could be precisely controlled by the voltages. The number of generated gray scale depends on how many voltage levels could be provided by the driving circuit and the transition characteristics of the cholesteric texture. This method was proven to be effective and the created gray scales are high quality and distinct. However, this driving method requires too many voltage levels for various gray scales which will tremendously increase the cost of the driving chip. Besides, high voltage DAC needed in this driving scheme would inevitably increase the design complexity.

4.2.2 RMS Control Method

As an alternative but effective method, the voltage field could also be controlled by the duty cycle and high and low positions of the driving waveforms. When the waveform is adjusted in the row and column lines of the cholesteric LCD, the overlapped cross pixel`s root of mean square voltage value will be varied which will lead to different gray scales. The challenge of this method is the design of the effective waveform pattern in all of the driving phases to ensure not only the correct switching but also the constant RMS value in the holding phase. By adopting this theory, we have created gray scales in the proposed dynamic driving scheme.

4.3 Gray Scale's Generation in the Enhanced DDS

4.3.1 Gray Scale's Generation by RMS Control Method

Since the resolution of the Ch-LCD increases quickly, high speed driving scheme with gray scale's capability becomes more important. Considering the dynamic driving scheme has the unrivaled driving speed, the generation of the gray scale within the dynamic driving scheme is highly desirable. In this part we will talk about the gray scale's generation method in the dynamic driving scheme.

It is known that the percentage of the transition from the homeotropic to the transit planar depends on the RMS values of the applied voltage filed during the selection and holding stages in the dynamic driving scheme. So, the method for switching of the effective voltage field in certain driving phases is critical.

As we have elaborated before, the PHM driving method could achieve gray scales in Ch-LCD but requiring many accurate high-voltage levels delivered by the driver circuit makes it unrealistic. As an alternative method, the RMS control of the electric field in the dynamic driving scheme by modifying the driving waveforms should be an effectual solution.

First let's observe the dynamic driving scheme we proposed in chapter 3 as shown in Figure 4-3.

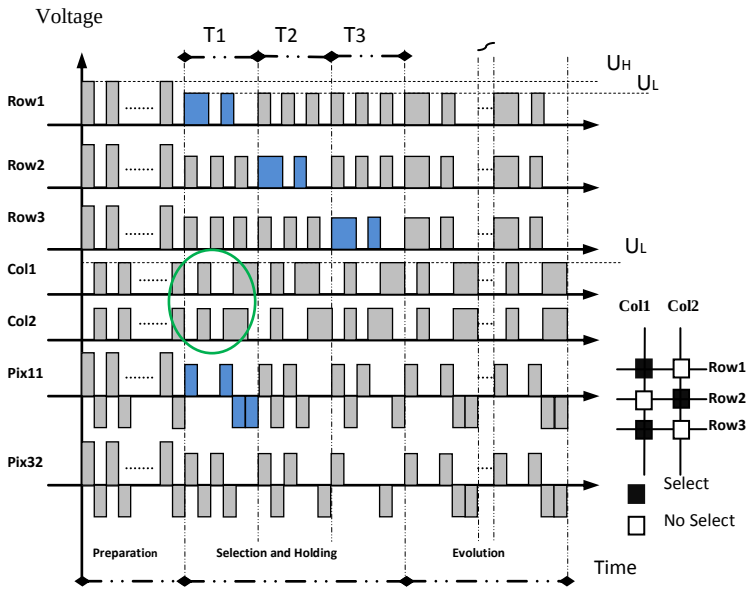


Fig. 4-3 Driving scheme of the enhanced dynamic driving

As an overview, the whole driving scheme of a 3×2 pixel matrix was illustrated in Figure 4-3. Column waveforms in the first selection stage T1 were marked by a green circle. When the first row is selected, the waveform in Row 1 remains unchanged. Nevertheless, the waveform in corresponding column lines (inside the green circle) has to be shifted in order to create different overlapped waveform patterns as well as different RMS values.

4.3.2 RMS Control in the Selection Stage

In order to elaborate the RMS control in the DDS, we divided a 40x40 panel into ten parts. Each part of it has four rows and 40 columns to display one gray scale.

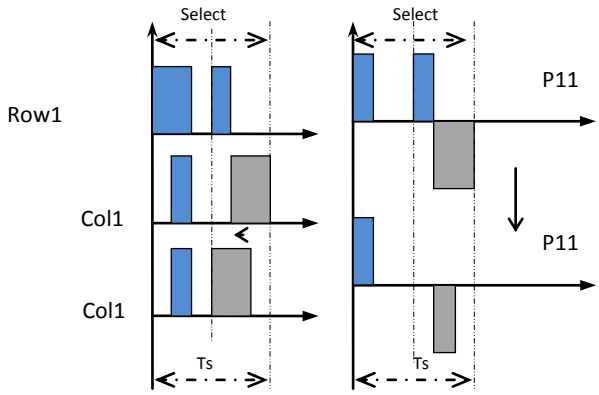


Fig. 4-4 Waveform of applied voltage field varies in the select stage

Figure 4-4 shows the sample of waveform in the selection stage for creating gray scales. It could be observed that when part of the column waveform varied, the cross pixel's waveform would change a lot. By adopting this method, the different RMS values can be generated because the duty cycle changes.

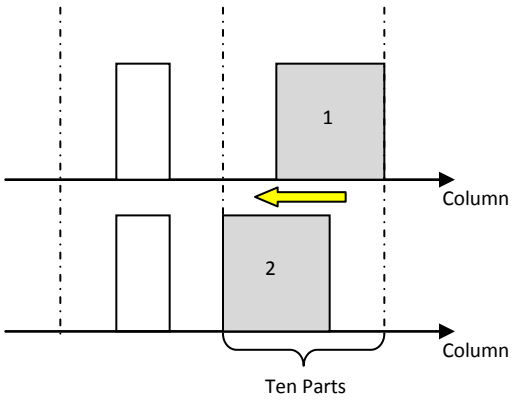


Fig. 4-5 Waveform moving for gray scale's generation in the enhanced DDS

Column waveform could be observed in Figure 4-5, the column waveform in the selection stage is made up by two parts. The right part of the waveform may be shifted from the end to the middle of this stage in ten steps (Position 1 to Position 2). We found out that starting at the 4th step, all further parts would lead to entirely off state pixels. So the switching region can be determined. Then the waveform was keep moving until the pixels were switched from dark to bright and the shift of RMS values were calculated.

The RMS value of the applied electric field in the selection stage can be calculated according to the following equation:

$$V_{rms} = \sqrt{\frac{V_1{}^2T_1 + V_2{}^2T_2 + \cdots V_n{}^2T_n}{T_s}}$$

$$= V_L\sqrt{\frac{T_1 + T_2 + \cdots T_n}{T_s}} \qquad 4\text{-}1$$

T_1, T_2… T_n are time period of each pulse when $U \neq 0$.

In the Equation 4-1, T_s is the total selection time needed to drive one row in the driving scheme, while T_1 to T_n are the durations of the voltage V_L across the selected pixel.

From our experiment above we found that the switch from dark to bright starts from the fourth part. The RMS values could be calculated according to Equation 4-1 which is between 30.26V and 31.47V with a selection time of 1.2ms. This means that the shift of the high level part is to be placed between 0.65ms and 0.72ms in the selection stage. The duration of V_L divided by the selection time should be between 0.54 and 0.6 as could be observed in Equation 4-2.

$$0.54 < \frac{TL}{TS} < 0.6 \qquad 4\text{-}2$$

Results from Equation 4-2 means that during the selection phase of the DDS, if the duration of cross pixel voltage level V_L divided by the selection time is varied within this time range, different gray scales could be generated.

Several experiments have been executed to verify this diving method in a cholesteric LCD demo panel provided by AEG MIS.

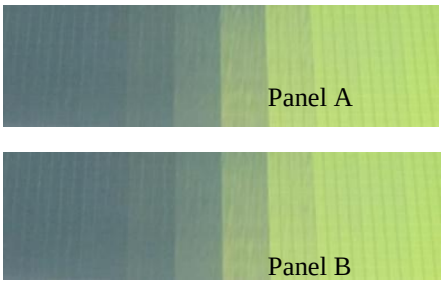


Fig. 4-6 Gray scales created by the RMS control in the enhanced dynamic driving scheme

As shown in Figure 4-6, distinct gray scales have been successfully created by the RMS control method in the enhanced dynamic driving scheme. The driving method was also executed twice in different area of the cholesteric panel demonstrating that the gray scale generation is stable and reproducible.

Besides, comparing to the two-value driving of the cholesteric LCD, the constant RMS value in the holding stage is more important.

4.3.3 Constant RMS Value in the Holding Stage

Since the cholesteric LC is quite sensitive to the RMS values of the electric fields during the selection stage in DDS. The holding waveforms after the selection phase must guarantee that the cross pixel's RMS value remains unchanged while the RMS value in the selection phase is varied. This would ensure that the holding waveforms do not affect the function of the driving. This is especially important for gray scale driving because the required RMS values in the selection phase change frequently.

4.4 Multi Selection Method for More Gray Scales

4.4.1 Two Selections Method

The number of grayscale generated by the RMS control method in the enhanced dynamic driving scheme is limited and in the range of 10, as shown in Figure 4-6. In order to explain the reason of this limitation, we'd better go back to the characteristic of the cholesteric material.

Figure 4-7 shows the reflectance versus voltage curve at 50 Hz driving frequency. As depicted in this plot, in the dynamic driving scheme, when the pixel was selected from pre-prepared homeotropic state to the bright planer state or dark focal conic state through the meta-stable transit planer state (depicted by a black arrow), the transition is quite steep as the curve marked by the yellow arrow. This intrinsic characteristic of this texture means that the reflectance will change very fast, when the effective driving voltage field is shifted in the selection stage. It makes the RMS control for different gray scales too sensitive. Such a steep characteristic of the cholesteric texture is a big obstacle for enlarging the grayscale numbers in the dynamic driving scheme.

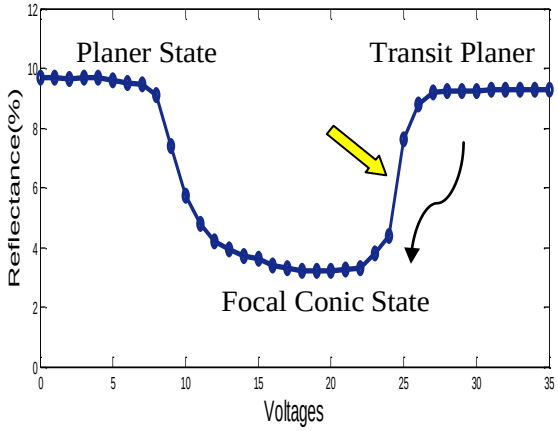


Fig. 4-7 Reflectance of the Ch-LCD vs. applied voltages

As we talked above, in the dynamic driving scheme we proposed, we adopted the method by controlling the waveform pattern in the selection part to generate expected RMS voltage values as well as different gray scales. Since the transition is quite steep as shown in Figure 4-7, the precisely RMS control in the selection stage needs to divide the driving waveform into many sub-parts to accurately match certain values. This would be easy to explain if we zoom in part of the transition curve as shown in Figure 4-8.

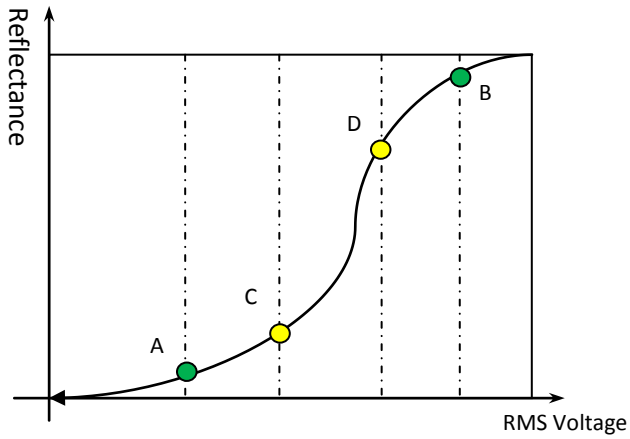


Fig. 4-8 Fraction of the R-V curve

Figure 4-8 shows an enlarged part of Figure 4-7 which is marked by a yellow arrow. Letter A, B, C and D on the curve represent different gray scales with certain reflectance. When the waveform is shifted in the selection part of the driving scheme, it will yield to certain RMS values. For instance, gray scales A and B could be created in this way. However, if we want to further increase the gray scale's number, such as creating gray scale C and D on the curve, we have to further divide the waveform for more sub-parts to match these RMS values as well as generating new gray scales.

Since we know from above that the transition from homeotropic state to other states is steep as shown in Figure 4-7, the further division of the driving waveform will require high driving frequency. However, it will also suffer from other problems. One of them is the frequency induced parameter drift.

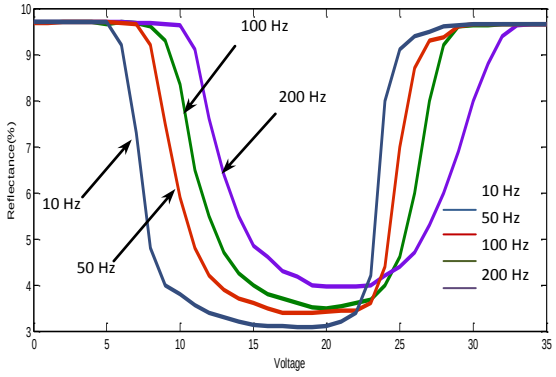


Fig. 4-9 Reflectance vs. voltages of the Ch-LCD at different driving frequency

Figure 4-9 shows reflectance curves vs. applied voltages measured at different driving frequency. As shown in this Figure, the maximal contrast ratio varies with the driving frequency which ranges from 10 Hz to 200 Hz. It could be observed from Figure 4-9 that the transition curve will shift

when different driving frequency is chosen. If the driving frequency varies too much, the resultant values will be obvious affected.

Furthermore, the driving frequency will affect the threshold voltage for switching between planer and focal conic states at both sides. The reflectance curve moves to the right side if the driving frequency is increased. At the lower voltage side of the curve, the voltage which will not affect the pre-prepared planer pixels could be higher when the driving frequency gets higher. Thus, if the contrast ratio is good enough, the driving frequency could be set higher to allow more sub divisions. The high voltage in the scan lines during the selection time could also be reduced if higher voltage is used in the data lines. This may reduce the cross pixel's voltage field of the no select pixel and the planer pixels will be less affected by the upcoming holding waveforms.

The contrast ratio also has correlation with the driving frequency. The lower driving frequency leads to a higher contrast ratio. However, the lower driving frequency also means less grayscales and may damage the cholesteric texture if too low.

On the other side, higher driving frequency also add extra burden to the driver chip which also could be a deficiency of such a solution.

The method we talked above has so many limitations in increasing the number of gray scale in the enhanced dynamic driving scheme. Therefore we want to introduce a novel method called Multi Selection Method (MSM) as an alternative but effective solution to solve this problem [36]. As the name indicates, the multi selection method is to select the display pixels more than one time in the driving scheme which is different from the one selection method in the former dynamic driving scheme. In order to better explain how this method works, we use Figure 4-10 to illustrate.

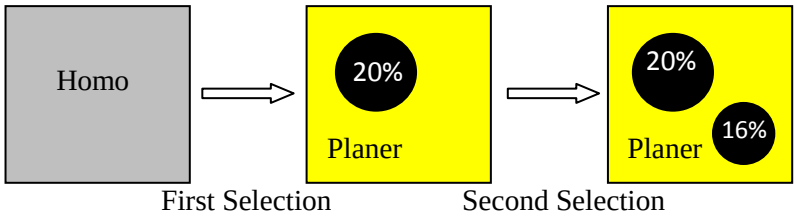


Fig. 4-10 Illustration of two selection method

Figure 4-10 illustrates a schematic of the two selection method in the dynamic driving scheme. In the DDS, the preparation stage will firstly refresh all pixels into the homeotropic state. After that, the homeotropic state pixels will be selected to pure planer or focal conic state and of course the mixed state gray scales. In the first selection stage, as the example in Figure 4-10, 20% of the homeotropic texture in a pixel was selected to the focal conic state while the other 80% of the texture is changed to the planer state. Thus, a gray scale which has 80% of the reflectance of a pure planer state pixel is created. Next step, in the second selection stage, the gray scale created by the

first selection stage was selected once more. Let's say the RMS values in both of the two selection stages are the same then extra 16% of the original planer texture of the pixel will be selected to the focal conic state. That's to say, under the same driving conditions, a new gray scale who has the 100% - (20% + 16%) = 64% reflectance of the pure planer pixel could be created. The only shortcoming of the multi selection method is the longer driving time comparing to the one selection method for executing two or more selection stages. However, please note that the selection stage in the enhanced dynamic driving scheme only takes around 1 millisecond per row. For controlling a 100 lines cholesteric display, 0.1 second extra driving time is totally acceptable. Therefore, the cost of the method, longer driving time, is acceptable.

To put the multi-selection theory into reality, we imbed it into the enhanced four stages dynamic driving scheme. According to this method described above, the two selections are arranged in series after the preparation stage, as illustrated in Figure 4-11.

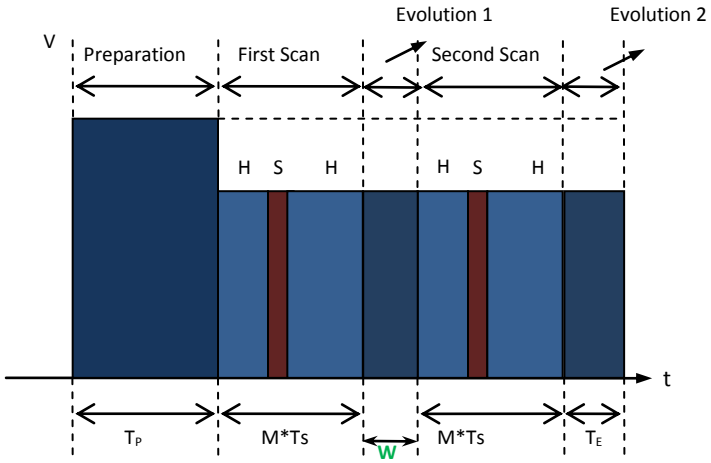


Fig. 4-11 Driving sequence of a four stages two selections dynamic driving scheme

Figure 4-11 shows the driving sequence of the two selections dynamic driving scheme and the w here is the width of the first evolution stage for the first selection frame. The cholesteric display will be scanned twice for more gray scales at a lower driving frequency. After the pixels are in the homeotropic state, the first selection frame is the same as that in the one selection method and another selection frame is added once again after the first scan of the whole display completed. The independent two selection stages could be adjacent without any gap (w=0) because the cholesteric texture which are supposed to be selected to the planer state will be keep on the homeotropic state during the period of the two scans. When all parts of the driving scheme are passed, the maintained homeotropic texture will switch to the planer state immediately. That's the reason that two scans after the preparation stage could be put adjacent without any gap.

The width of the evolution stage in the first scan of Figure 4-11 could also be introduced and optimized. As we know that in a normal dynamic driving scheme, selecting one row takes around 1

millisecond to finish. In the two selections method, if the controlled rows of the display are larger than 12 lines, the holding part before the selection part in the second selection stage could behave as an evolution part for the last several rows in the first selection stage. Therefore the evolution stage needs only once after two selection stages to ensure the last several rows of the display could completely be switched to the focal conic state and the total driving time will be reduced. In the practical side, the rows of the display will be of course more than 12 lines. Thus, normally the timing sequence of the two selections method in the dynamic driving scheme could be simplified to Figure 4-12. From Figure 4-12 we could observe that in the whole driving scheme, the preparation and evolution stages are performed just once. The selection and holding stages need to repeat twice which will add only 1ms per line to the whole scheme.

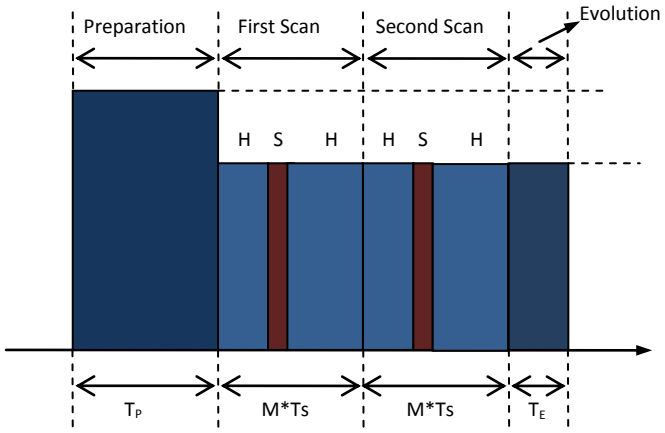


Fig. 4-12 Optimized driving sequence of a four stage two selection DDS

To verify this theory, we have implemented a two selections driving scheme into a 20 lines cholesteric LCD panel with only one evolution stage in the rear of the waveform sequence. Achieved result shows that the last several rows of the display could successfully be switched to the correct state. This also proves that only one evolution stage is enough in the two selection method to control more than 12 lines' display.

To execute the two selections method for gray scale's generation in details in the waveform side, here we give an example of the waveform in the dynamic diving scheme we have proposed in the last section. The waveform patterns in the selection and holding stages have been designed to have the ability for both the on-off driving and the gray scale driving.

In this two selections method only three voltages are used in the whole scheme. The waveform in the selection, holding and evolution are designed according to several rules.

First of all, the overlapped row and column waveforms in the selection stage should ease the control of the RMS values in this stage. In every selection stage, the row and column waveform is divided into six divisions. The six divisions of the waveform have the advantage that it will

maximize the use of the applied voltage. The RMS values could be higher even in the same applied voltages, so that the voltages could be reduced. As to the holding stage, the overlapped row and column waveforms should always have the same RMS values in every row. This is very important because the stable RMS in every holding part will let the holding waveforms be neutral and do not affect the selection stage. That is also to say, wherever the selection part is, the holding parts before and after will always in a stable RMS value, no matter how many holding parts are.

Besides, for the same reason, the waveform in the holding and evolution stages also need to have the same RMS value to make sure the last several rows will not be affected by the random fluctuation of the RMS values after it was selected. In order to fulfill these rules, the designed waveforms in the selection and holding stages are illustrated below.

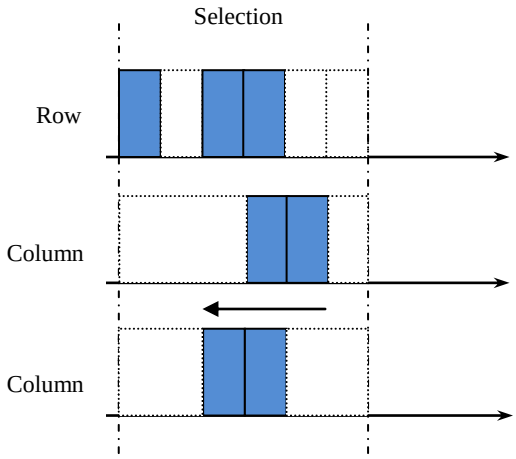


Fig. 4-13 Row and column waveforms in the selection stage

Figure 4-13 shows the waveform in one selection stage. Since the gray scale's generation region in the dynamic driving scheme is quite narrow, therefore we should firstly make sure in which region the gray scales could be achieved. The driving voltages used in the scheme are 48v, 38v and zero.

We could calculate that when the column waveform is in position one (upper column of Figure 4-13), the cross pixel's RMS voltage value is

$$V1 = V_L \sqrt{\frac{T_1 + T_2 + \cdots T_n}{T_s}}$$

(T_1, $T_2 \ldots$ T_n are time period of each pulse when $U \neq 0$.)

$$= 38 \times \sqrt{\frac{1}{2}}$$

$$= 26.9 \text{ volt}$$

And when the column waveform is in position two in the left side (upper column of Figure 4-13), the cross pixel's RMS voltage value is:

$$V1 = V_L\sqrt{\frac{T_1 + T_2 + \cdots T_n}{T_s}}$$ [T_1, T_2… T_n are time period of each pulse when U≠0.]

$$= 38 \times \sqrt{\frac{1}{6}}$$

$$= 15.5\text{volt}$$

Therefore, when the column waveform is moved from the right side position one to the left side position two, the RMS value will vary in the region:

$$15.5\text{ v} \leq V_{RMS} \leq 26.9\text{ v}$$

Thus, the gray scales could be created by the RMS voltage values generated by the overlapped row and column waveform patterns in the selection stage.

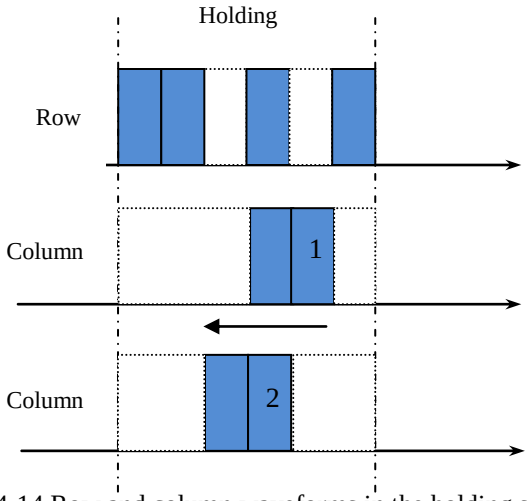


Fig. 4-14 Row and column waveforms in the holding stage

The row and column waveforms in the holding stages both before and after selection stages are illustrated in Figure 4-14. As we could observe in Figure 4-14, when the column waveform moving from the right side to the left side to create gray scales in the selection stage, the waveform pattern could insure that the cross pixel's RMS voltage values are not altered.

The RMS voltage value of the holding stage could be calculated through the equation below:

$$Vhold = V_L\sqrt{\frac{T_1 + T_2 + \cdots T_n}{T_s}}$$ [T_1, T_2… T_n are time period of each pulse when U≠0.]

$$= 38 \times \sqrt{\frac{4}{6}}$$

= 31.02 volt

We could observe that the holding voltage is high enough to hold the unselected homeotropic textures remaining in their state until the selection or evolution stage starts.

The design of waveform in the evolution stage could be flexible. Waveform pattern only needs to have the same RMS voltage value as in the holding stage. Therefore we choose a typical evolution stage's waveform from dynamic driving scheme.

After the waveform pattern of every stage has been developed, we can draw the complete driving waveform of our two selections dynamic driving scheme as illustrated in Figure 4-15.

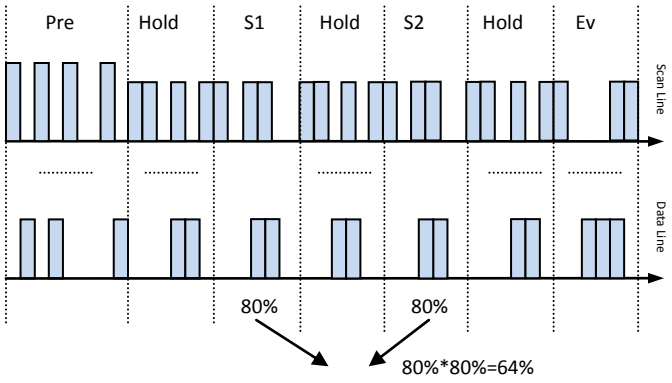


Fig. 4-15 Completed driving waveforms with 2 selections

As described in Figure 4-15, the preparation phase was followed by two selection stages S1 and S2 and the holding stages were arranged before and after S1 and S2. The prepared homeotropic state of cholesteric texture will be partly selected to the transit planer state in the first selection S1, and other homo state material will be held until the second selection S2 starts. There is only one evolution stage needed in this method. The series two selections combined can achieve many middle RMS values as well as more gray scales even at a lower driving frequency. The only drawback of this method is that the selection time would be longer. However, considering that the application of the Ch-LCD usually does not need to refresh very often, the extra 0.1s driving time for a 100 lines display is not a big deficiency.

In each selection, the RMS voltage value can be control to get certain percent of the focal conic texture. The two different values of each selection then will be combined to create a new gray scale. The RMS voltage value could have many combinations. As in our test waveform, the waveform in the selection stage was divided into 10 divisions. The combinations of two selections are in the table below.

Gray Scale	Selection 1	Selection 2	Planer (%)
1	0	0	100%
2	0	1	92%
3	1	1	85%
4	1	2	70%
5	1	3	45%
6	0	2	32%
7	0	3	21%
8	0	4	12%
9	1	4	5%
10	9	9	0%

Table 4-1 Combination of the waveform positions in two selections

It has to been noticed here that final gray scale is independent with the sequence of the two selections, which means, for instance, combinations of 7-2 and 2-7 in two selections will yield to the same gray scale.

Experiment to validate this grayscale generation method was executed in a 20×40 Ch-LCD demo panel adopting different driving schemes. Figure 4-16 (A) shows the grayscales generated by the dynamic driving scheme with 1-selection. The waveform in the column lines has 20 divisions of the RMS region, which means the ratio of high voltage time to selection time is changed from 3/6 to 1/6 in 20 steps cross a selected pixel in the selection stage. As we talked in the last page, in this region, the gray scale could be generated. Figure 4-16 (B) is the generated gray scales using the 2-selection dynamic driving method with the same waveform divisions.

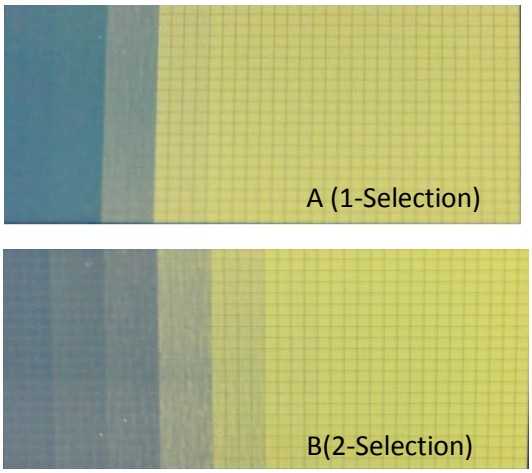


Fig. 4-16 Comparison of the grayscales generated by 1-selection and 2-selction methods

By comparing the gray scales generated by one selection method with those generated by two selections method, it's easy to find out that the gray scale number have been increased in the dark side and the contrast ratio was not reduced at the same time. This has proven that the multi selection method is effective to create more gray scales under the same driving conditions. This also means the resolution in the dark side has been expanded which fits well with the gamma function where dark gray values need to be dissolved in higher linear densities than the bright gray values.

4.4.4 Three Selections and More

The selection also could be extended to three all more in the purpose of creating more gray scales. The waveform below shows the three selections method in the enhanced dynamic driving scheme. Details of the waveforms are the same as those in the two selections method.

As shown in Figure 4-17, the selection was executed three times in the dynamic driving scheme. Considering the number of RMS values' combinations in three selections is an exponential comparing to that in the two selections method, the complexity will be largely enhanced. The resulted HW cost will also increase. Such a high gray scale resolution may be make more sense for future Ch-LCD with better physical characteristics like higher contrast ratio.

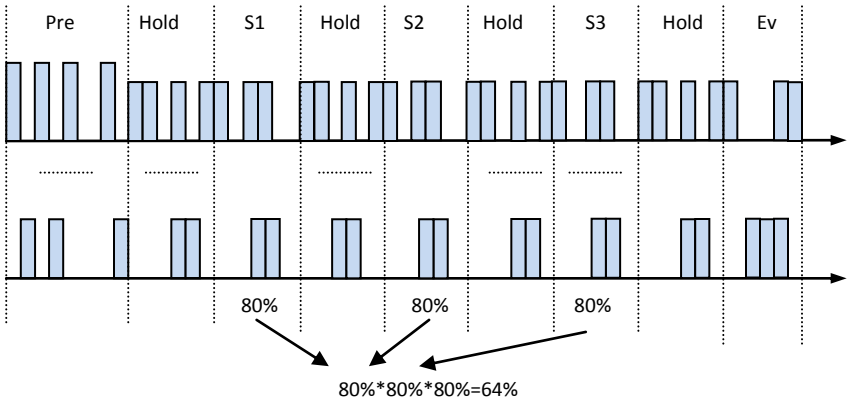


Fig. 4-17 Completed driving waveforms with 3 selections

Experiments about three selections pattern were also executed at the same driving frequency, the perceivable number of generated grayscale is a few more than that of the two selections scheme. Considering the limitation of the cholesteric material and the extra time needed for driving, the two selections scheme is recommended.

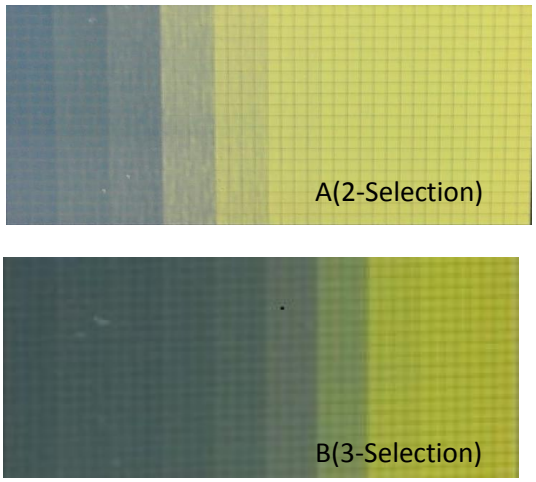


Fig. 4-18 Comparison of the gray scales generated by 2 and 3 selections methods

Figure 4-18 shows the comparison of the two and three selections method for gray scale's generation. We can observe the number of the gray scales generated by the three selections method is a little more than that generated by the two selections method. Thus, for the gray scale's generation of today ́s CH-LCD, two selections method is a tradeoff choice for more gray scale number as well as short driving time.

4.5 **Conclusion**

- Number of Gray Scales

The gray scale generated by the RMS control method in the selection stage of the enhanced dynamic driving scheme has been proven to be applicable. Multiple gray scales could be achieved without adding complicated driving chips. Because of the steep transition in the R-V curve, the number of the generated gray scale is limited even by using the multi selection method at the cost of longer driving time.

- Uniformity of the Gray Scale

Uniformity of the generated gray scales by adopting the enhanced dynamic driving scheme is still not satisfactory. Figure 4-19 shows the generated gray scales in a 40×40 demo board of cholesteric LCD by adopting the two selection method with 10 divisions of the waveform in the gray scale region.

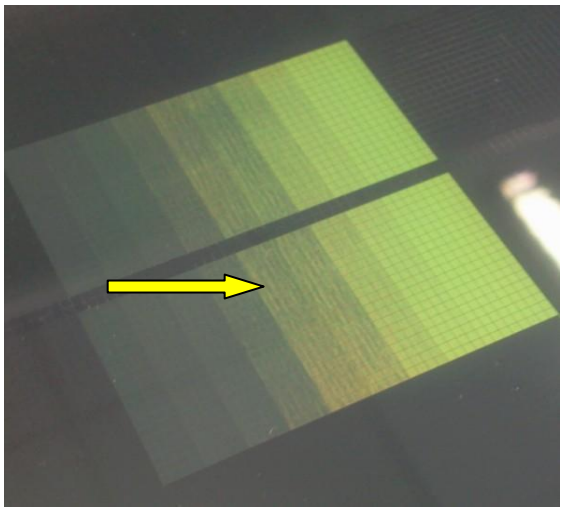


Fig. 4-19 Gray scales generated by using the multi selection method in the proposed dynamic driving scheme

From Figure 4-19, besides the various gray scales, we also could observe that the uniformity of the generated gray scales is not satisfactory, which has been known as a drawback of Ch-LCD. Inside one of the mid tone gray scale the uneven distribution of planer and focal conic textures is clearly visible. This could be the reason that the transit from the instable transit planer to the stable state is fast and may easily be disturbed. During our test we also found that the gray scales generated by RMS control in the diverse dynamic driving methods all have similar problem. Therefore we have reasons to believe that the non-uniformity of the gray scale is caused by inherent characteristic of the dynamic driving scheme.

In order to improve the uniformity of the gray scale, in the next chapter we would propose a newly designed driving method making use of the static transition from static planer state to the focal conic state in a relatively fast driving speed in which better gray scales may be expected.

5 Novel Fast Static Driving Scheme for Uniform Gray Scale

5.1 Introduction

In the last chapter we discussed that the gray scale's generation in the dynamic driving scheme by the RMS control has intrinsic drawbacks which are the limited number of gray scales as well as the observed non-uniformity inside one gray scale tone. In the driving of cholesteric LCD, the switching from planer state to focal conic state is quite fast, usually needs about 1ms to complete [37]. However, switching from focal conic state to planer state requires much longer time, which becomes an obstacle in fast driving of Ch-LCD. That is also the reason that the dynamic driving scheme was introduced to achieve a fast driving speed by firstly driving all of the pixels into a homeotropic state and then the homeotropic will be held during the whole driving time until the selection stage starts. However, since the switch from the planer state to the focal conic state is quite fast, if we could find a method to control the display by firstly switching all of the pixels into the stable planer state, then it will be possible to select pixels into the focal conic state at a fast driving speed. The other important aspect of such a new driving method we must care here is that the unselected planer state pixels must not be affected during the selection of the focal conic pixels to ensure the high contrast ratio.

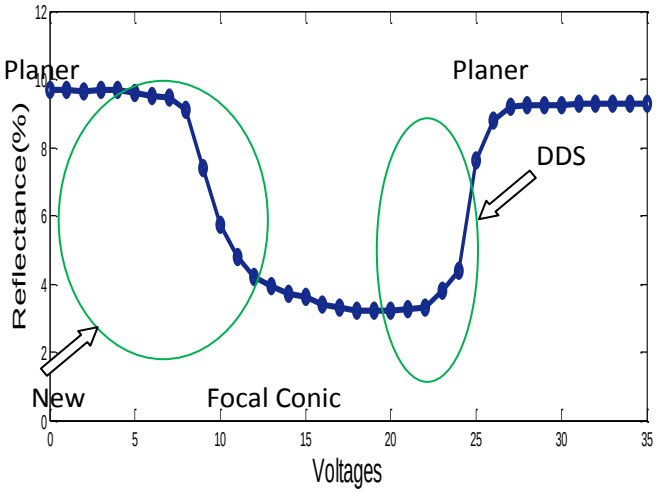


Fig. 5-1 Gray scale region of reflectance of the Ch-LCD vs. applied voltages

On the other side, as depicted in Figure 5-1, the transition from the planer state to the focal conic is smooth in the left side of the R-V curve comparing to the transition in the right side which is used for the gray scale generation in the enhanced dynamic driving scheme. Thus, if we could find a

method to create gray scales by using the left side transition of the Ch-LCD, number of the created gray scale could be larger.

By adopting these considerations above, the new driving scheme which is making use of the smooth left side of the R-V curve could be illustrated in Figure 5-2. [38]

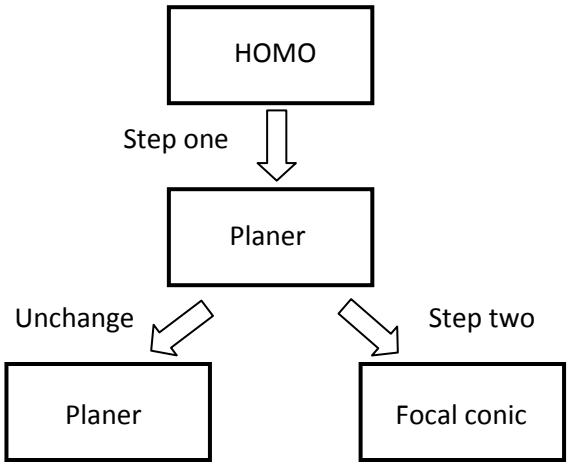


Fig. 5-2 Driving principle of the new static driving scheme

Figure 5-2 shows the driving principle of the new driving method named fast static driving scheme. As we could observe in Figure 5-2, all pixels are firstly selected to the homeotropic state which is the same as that in the dynamic driving scheme. However, unlike that in DDS, the prepared homeotropic state texture will not be kept but all be switched to the planer state directly which is the step one of Figure 5-2. After all the pixels are in the stable planer state, some of the pixels could be switched to the focal conic state and others could be left unchanged. According to the principle explained before that the switching from the planer state to the focal conic state is quite fast, therefore the driving speed of this method would be considerably higher than the conventional static driving scheme.

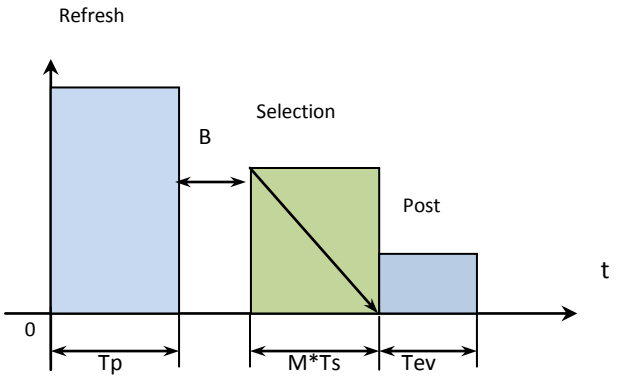


Fig. 5-3 Driving sequence of the new driving scheme

Figure 5-3 shows the driving sequence of the proposed fast static driving scheme. The new driving scheme has three stages which are named refresh, selection and post stage. The refresh stage is to refresh all of the pixels firstly into the homeotropic state, then the applied voltages will be turned off immediately and the zero voltage will be last for a while, which is aimed to let the homeotropic texture fully switch to the stable planer state. The refresh stage should be strong enough to switch all of the pixels to the brightest fully planer state in order to get the highest contrast ratio. After all of the pixels are in the stable planer state, the selection stage starts to scan the display line by line to select certain pixels into the focal conic state and leave the unselected pixels staying in planer state. At the end of the selection stage, a short post stage is added to make sure that pixels in the last several rows get enough time to fully evolve into the focal conic state.

5.2 Driving Times of Each Driving Stage

5.2.1 Length of the refresh stage

For the realization of this driving scheme, according to the three critical stages depicted in Figure 5-3, choosing the proper length of each stage is of great importance. The refresh stage is aimed to drive all of the pixels into the homeotropic state which has the same function as the preparation stage in the common dynamic driving scheme. Since we have introduced this in details before, through experiments in our lab, 35 volts alternative voltage field lasting for 45 milliseconds has been chosen.

5.2.2 B (Blanking) between the refresh stage and selection stage

The second one we have to concern is the length of the gap between the refresh stage and the selection stage which was marked in Figure 5-3 by B. The refresh stage cannot be directly followed by the selection stage because the transition from the homeotropic stage to planer stage may not be finished when the refresh waveform ends. In the dynamic driving scheme, because the selection waveform starts to select directly from the maintained homeotropic stage, the gap between the preparation stage and the selection stage could be zero. However, in this new driving scheme we are describing here, the selection stage should start to work when all the pixels are already in the stable planer state. Therefore, after the refresh stage, the blanking time B has to be spent to get the transition completed.

Since the achieved planer state texture will not change if no extra voltage field is added, the length of B in which duration the voltage applied across the pixel is zero may be very long. For optimizing the driving time, experiment was executed to find the shortest length of B. We have found through the tests on a cholesteric display panel, B should be selected to a value more than 15 milliseconds. Therefore the length of 20 milliseconds should be long enough to get the stable planer state. Although the transition from the homeotropic state to the planer state should be very

fast, the B still needs to be several times longer than the transition time to avoid that the transition in some of pixels is not fully finished.

5.2.3 Length of the selection stage

Since the display will be scanned line by line in the selection stage, the length of the selection stage would be increased when more lines are controlled. For a display panel with m lines, the length of the selection stage should be m × Ts. The parameter Ts is the selection time to drive one line. The selecting from the planer state to the focal conic state should be around 1 millisecond. 2 ms for the length of Ts has been chosen because the driving scheme is designed to have the ability to both, the binary (on/off) driving as well as the gray scale driving. Experiments of the gray scale driving had shown that the quality of the gray scales were not good at around 1 millisecond about which will be discussed below.

5.2.4 Length of the post stage

Similar to the function of the evolution stage in dynamic driving scheme, when the pixel is selected to switch to the focal conic state, the transition will not finish immediately. The lower voltage field must be kept for a while to ensure the transition to finish. In the new fast static driving scheme, pixels which are selected to the focal conic state in the last several rows need a constant low voltage field to evolve to the stable focal conic state. One thing which is different from the dynamic driving scheme is that pixels in the new driving scheme are selected from the stable planer pixels but not homeotropic state pixels. Therefore the length of the post stage may be a little different from that in the dynamic diving scheme. By testing the length of this stage from zero to 50 milliseconds, we found that by using our proposed driving waveforms, 15 milliseconds would be long enough to drive. Lengths longer than 15 milliseconds still work but are not necessary.

As a summary, the optimized lengths of each driving stage in the new driving scheme are listed in the table below:

Stages	Length
Refresh	50 ms
B(Blanking)	20 ms
Selection	2 ms
Post	15 ms

Table 5-1 Lengths of the stages in the new static driving scheme

The critical lengths of the driving stages listed above are the minimum and optimized lengths needed in the gray scale driving of the Ch-LCD. The longer driving duration could also get the same image quality but is not necessary.

5.3 Waveform Patterns of All Driving Stages

To realize the new driving scheme, we have to design the driving waveforms to fulfill all of the expected design rules. Figure 5-4 shows the waveform pattern we used in the new driving scheme.

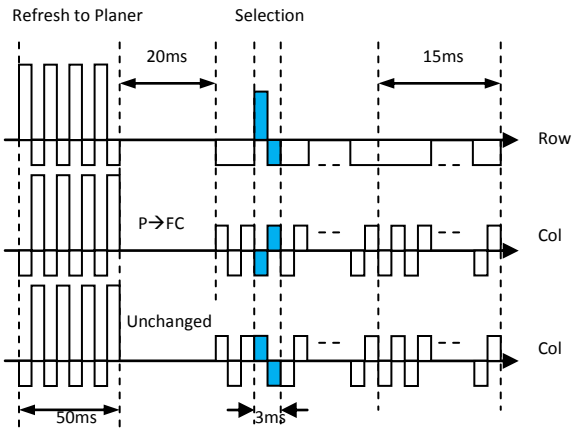


Fig. 5-4 Waveforms of the new scheme of Ch-LCD

As could be observed in Figure 5-4, in the refresh stage, the high and low voltages are alternative switched and the waveforms in row and column lines differ from half of the phase. So the cross pixel's waveform will be constant high voltage field to drive all of the pixels into homeotropic state.

In the selection stage, waveform in the row lines is kept in a small negative voltage unless it is the time to select this row. When one row is selected, half of the waveform in the selection stage will become a higher voltage to select the planer pixel into the focal conic state. The column waveform in the selection stage will be alternative low voltages with the opposite phase as illustrated in Figure 5-5.

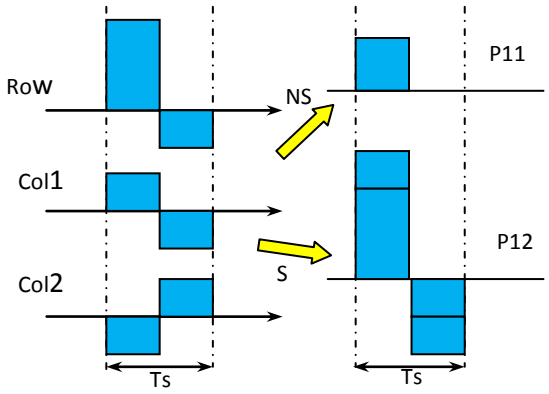


Fig. 5-5 Waveforms type for selection and non-selection

As we shown in Figure 5-5, when row and column waveforms have the same phase in the selection stage, the overlapped voltage field will be a lower voltage field applied on the pixel. On the other side, when row and column waveforms are in the opposite phase, the overlapped voltage field will be a higher voltage field to select the pixel from planer state to the focal conic state.

The cross pixel's driving waveform in the post stage will let the transition from planer to focal conic state to get fully completed in the last several rows. Besides, the waveform also has to make sure that the non-selected planer state pixels would not be affected.

5.4 Voltage Values of the Driving Scheme

As we have described before in details, all of the pixels are first refreshed to the planer state by a 50ms bipolar waveform followed by a 20ms blanking time to make sure that the cholesteric texture is fully switched to the stable planer state. When the stable planer state is established, the display will then be selected line by line at about 2ms per line for a good contrast ratio. The higher voltage is only used in the selection time of each line to drive the aimed pixels into the focal conic state. There is no need to hold the homeotropic state in the whole driving time. The data line signals of low bipolar voltages to get less crosstalk. After the selection stage, the lower bipolar voltages will still last for 15ms to ensure the focal conic pixels in the last several rows staying stable. In order to understand these rules, let ś first have to look into the inner characteristics of the cholesteric material.

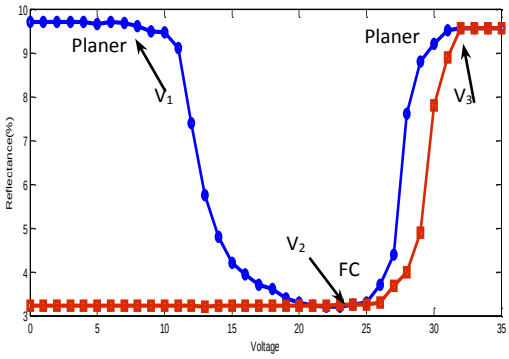


Fig. 5-6 Reflectance vs. voltages of the Ch-LCD

Figure 5-6 shows the reflectance vs. applied voltages curve of the Ch-LCD. It can be observed from Figure 5-6 that V_3 is the threshold voltage to refresh the display into planer state while voltage field around V_2 could drive the planer pixels into focal conic state. The applied voltage below V_1 will have no effect on the planer pixels.

There are only 4 voltages needed in the whole driving scheme, which are 28v, 22v and ±7v. The 28v high voltage is only used at the first of the driving scheme to refresh all of the pixels into the

planer state. And the 22v is only used in the row selection time. The waveform pattern should guarantee the planer state pixel could be fully switched to focal conic state while the non-selected planer pixel will not be affected by the waveform. In order to achieve this, the root of mean square (RMS) value of the voltage field in the selected pixel should be around V_2 while the RMS value in the non-selected pixel should be lower than V_1. In our driving scheme, we use ±7v voltages pulses in the data lines. When the ±7v voltage pulses have the same phase as the selection pulse in the scan line, the overlapped voltage field will be high enough to switch the planer pixel into the focal conic state. On the contrary, when the phase of the ±7v pulses have the opposite position comparing to the row selection's phase, the cross pixel's voltage field will become low. By calculating of the RMS value of the cross pixel voltage, the value of the voltage in the unselected pixel is smaller than V_1, therefore the brightness will have no decrease on the planer pixels.

The new driving scheme was executed in a 40×40 cholesteric display panel as could be observed in Figure 5-7.

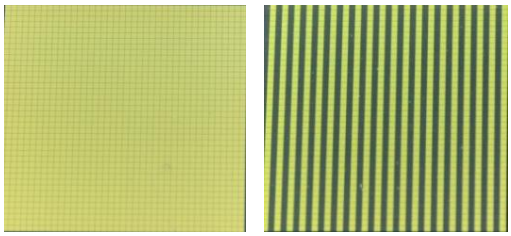


Fig. 5-7 Planer pixels without and with selection phase

In the left image of Figure 5-7, all pixels were only driven to the planer state without any followed selection and post waveforms. In the right photo the display was selected to dark every second column. From Figure 5-7 we can observe that the non-selected planer pixels are still bright in the right photo and the contrast ratio remains good.

Reduced Power Consumption

In the new fast static driving scheme, the highest driving voltage is only used in the first refresh stage to drive all of the pixels into the homeotropic state. After the refresh stage, the voltage field only gets higher in the short selection stage. Different from the dynamic driving scheme in which the higher voltage is always needed in the holding stage and evolution stage to hold the homeotropic state throughout the whole scheme, the new fast static driving method will consume less power than dynamic driving scheme. Furthermore, in the new driving scheme only one row is controlled at one time. So the power consumption of the new static driving scheme is lower than that in the dynamic driving scheme.

Fast Driving Speed

The new fast static driving method could achieve the driving speed close to normal dynamic driving scheme. In our experiments the driving speed could be achieved around 2 ms per line. This speed is much faster than the conventional driving scheme so that the fast static driving scheme is practical.

5.5 Gray Scale Control in the Fast Static Driving Scheme

A notable merit of the proposed new driving scheme is the generation of uniformed gray scales. As discussed in chapters 4, a deficiency of the dynamic driving scheme of the Ch-LCD is the generation of the gray scales. The gray scale number will be limited because of the intrinsic transition characteristics. Besides, the uniformity of the gray scales is also not satisfactory. In the new driving scheme, the gray scale is directly generated from the stable planer state instead from the transient planer state like the dynamic driving scheme, thus the uniformity will be largely improved. As could be observed in the R-V curve of Ch-LC, the left side of the R-V curve is not that steep comparing to the right side of it. Therefore this characteristic will let the gray scale's generation in the new driving scheme easier.

First we will introduce how we can control the waveform to generate gray scales. The control of the gray scale is actually to control the domain size of the planer texture in the cholesteric cell. [39]

Figure 5-8 shows the waveform's explanation about how the gray scale could be generated in the new driving scheme. During the selection time period of the new driving scheme, the position of the higher voltage pulse in the column lines varies from left side to the right side while keeping the high to low ratio unchanged. The movement of the column pulse will lead to change of the RMS value of the cross pixel's voltage field.

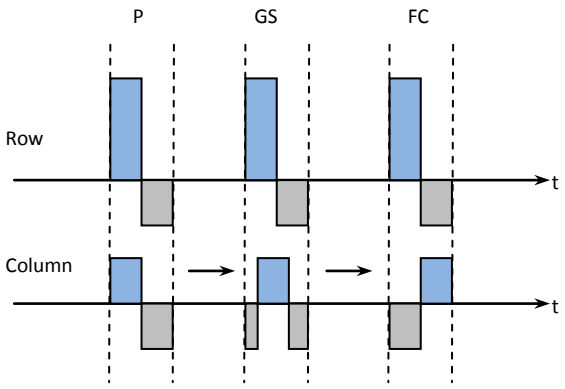


Fig. 5-8 Waveform moving for generating gray scales

When the movement of the waveforms matches certain RMS values in the left side of the R-V curve, the pre-prepared planer state pixel will be partly selected to the focal conic state and a different gray scale can be generated. The constant duty cycle of the data pulse during the whole

driving scheme could ensure the constant RMS values in the non-selected time which will be helpful for the uniformity of the generated gray scales.

Gray scale's generation by adopting this driving scheme was also executed in the display panel. The higher voltage pulse in the data lines is divided into 10 parts to move it from left to the right side as the waveform pattern depicted in Figure 5-8. When the waveforms move in certain region, different RMS values could be matched and several gray scales would be generated in test panel as shown in Figure 5-9.

Fig. 5-9 Grayscale generated by one selection method in the new scheme

The uniformity of the gray scales is considerably better comparing to those generated by the dynamic driving scheme (e.g. Figure 4-19). This may due to the static transition from the stable planer state to the stable focal conic state, while in the dynamic driving scheme the transition has to go through the meta-stable homeotropic state and transient planer state. Furthermore, comparing with the dynamic driving scheme, at the same waveform's division, more gray scales could be distinguished which indicates the gray scale is more easily to be generated in this scheme. Even at the same driving conditions, the gray scale resolution will be higher.

5.6 Multi-Selection Method in the Fast Static Driving Scheme

The multi-selection method as described in the 4.4 of the last chapter to get more gray scales without additional IC cost and complicated voltage levels could also be adopted here.

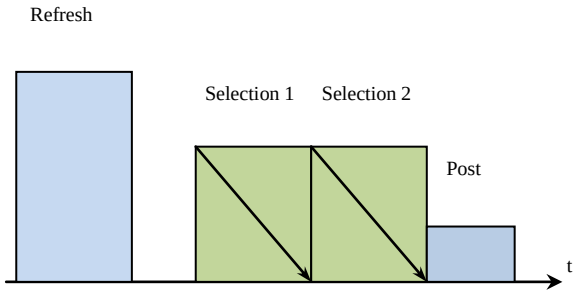


Fig. 5-10 Driving sequences of the two selections method

As described in Figure 5-10, this method is to select the display two or more times to get more middle tone gray scales. In our new fast static driving scheme, after all of the pixels were refreshed to the planer state, the whole display will be scanned twice before the post waveform starts to stabilize the last several rows. For instance, if during the first selection, 20% of the planer texture is selected to the focal conic state, in the second selection, the same driving waveform will switch 20% the left planer texture to the focal conic state. Therefore a new gray scale which includes 36% of focal conic texture will be generated without extra burden to the driver chip which could not be achieved by the one selection method.

A two-selection driving method was also adopted within the new fast static driving scheme to compare with the one selection method. More middle tone gray scales could be obviously observed in the test panel comparing to the gray scales generated by one selection method at the cost of longer driving time. Considering that the driving speed of this scheme is much faster than that of the conventional driving method, the extra time (<0.5s for refreshing a 160 lines cholesteric display) caused by this method is acceptable.

By adopting the multi-selection method at a cost of longer driving time, more gray scales could be distinguished at the same driving conditions. The right image in Figure 5-11 shows the generated gray scales in a 40×40 cholesteric display panel by combing different RMS voltage values in each of the two selection stages. The display was selected twice during the selection stage of the new driving scheme to achieve more gray scales. The waveform pattern and applied driving voltages are consistent with those in the one selection method. It could be easily observed from Figure 5-11 that the number of the gray scales has been increased comparing to the gray scales generated by one selection method in the left side. The uniformity of the generated gray scales by the two selection method is also good.

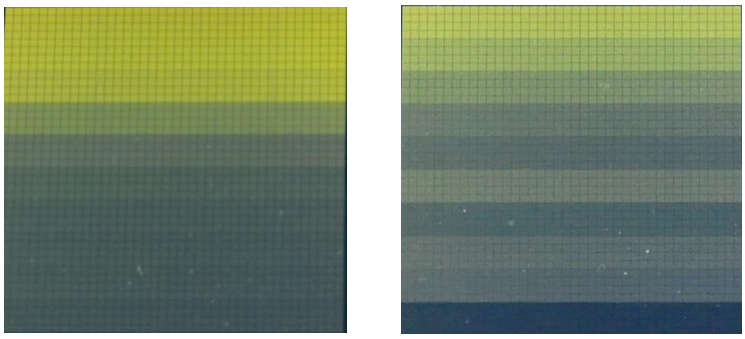


Fig. 5-11 Grayscale generated by one and two selections methods in the fast static scheme

More gray scales are also possible if three or more selection stages are added to this driving scheme. However, the driving time will inevitably become longer.

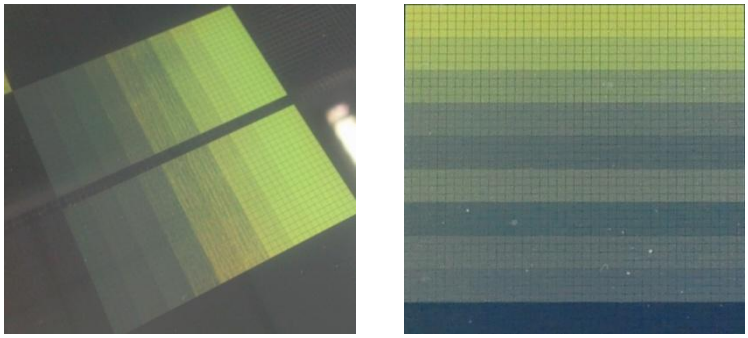


Fig. 5-12 Grayscale generated by DDS and fast static driving scheme

Figure 5-12 shows the compare of the gray scales generated by the enhanced dynamic driving scheme and the new fast static driving scheme. The left side image shows ten gray scales from the enhanced dynamic driving scheme we have proposed in chapter 3 and the right image shows the gray scales generated from the new fast static driving scheme. It is easy to find out that the uniformity of the gray scales is much better in the right image comparing with the left one.

5.7 Conclusion

In this chapter we have proposed a new fast static driving scheme for Ch-LCD. In the new driving scheme, which is different from that in the dynamic driving scheme, pixels are first driven to the stable planer state through the refresh stage and a predefined blanking time B. Then the selected pixels will be switched to the focal conic state by adding different driving waveforms. Since the generation of gray scale takes place at the left side of the R-V curve, compared with dynamic

driving scheme operating at the right side of the R-V curve, gray scale's number could be enhanced without adding hardware cost. The uniformity of the generated gray scale is also considerably better than those created in the dynamic driving scheme for the stable to stable transition.

6 Multiline Addressing of Ch-LCD

6.1 Introduction

In the active driving displays such as AM-LCD, each display pixel has a TFT circuitry to control the on-off of it. The TFTs behind pixels on the backplane allows a DC operation of the (RMS) voltages applied, so that every pixel of a high resolution display with many lines could individually be controlled. So addressing time of a row may be short and therefore improve the driving speed of the display. The Figure 6-1 shows the typical display matrix of an active driving display.

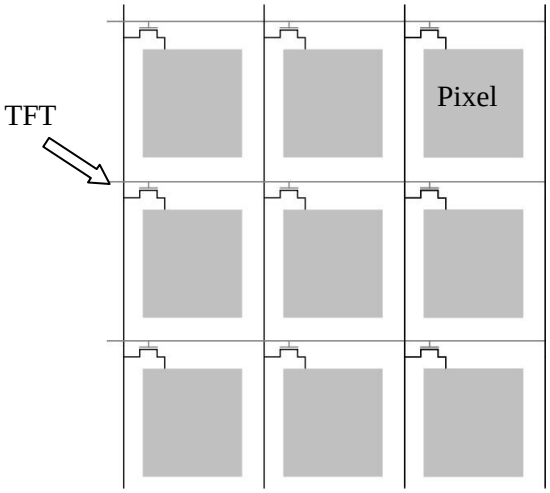


Fig. 6-1 Active driving display matrix

However, as to the passive matrix display, pixels of the display are scanned line by line to refresh the content and each time only one line could be controlled. An individual control signals is only effective during the addressing time of the row. The row addressing time is a reciprocal function of the number of the row. For high resolution display with many rows, it is hardly possible to generate different effective signals on the pixels, as in the most time, every pixel receives the same passive signal.

In order to overcome this limitation or to extend the display resolution, multiline addressing methods were invented for PM-LCD [40] and PM-OLED. [41] Let's consider the simplest case of multiline addressing. If only two lines are addressed simultaneously, the time needed for addressing a complete frame is halved. Or for the same frame period the row addressing time may be doubled. For PM-LCD the multiline addressing method may reduce the level of the voltage applied, so that the driver chip cost is reduced. For PM-OLED the current amplitude of an OLED pixel may be halved, so that the stress on OLED is reduced and the lifetime is increased.

Considering the driving speed is of particular importance in controlling of the cholesteric LCD, while no constant frame period as for video application is needed. So the multiline addressing method may largely increase the driving speed, especially when the resolution of the display gets higher.

The principle of multiline addressing of PM-LCD based on the orthogonal row signal and column signal. [42] For the pixel located in row i and column j, the voltage $U_{ij}(t)$ across a pixel is

$$U_{ij}(t) = F_i(t) - G_j(t) \tag{6-1}$$

$F_i(t)$ is the row voltage with period T and the $G_j(t)$ is the column voltage with period T.

$$G_j(t) = c\sum_{i=1}^{N} I_{ij}\, F_i(t) \tag{6-2}$$

I_{ij} is the pixel value in the location row i and column j. c is constant independent I_{ij}.

The LCD reacts to the RMS value of U_{ij}, so

$$\langle U_{ij}\rangle = \frac{1}{\sqrt{T}}\sqrt{\int_0^T U_{ij}^2\,(t)dt} \tag{6-3}$$

By substituting equations 6-1 and 6-2 into 6-3, the RMS value of U_{ij} could be represented as follows:

$$\langle U_{ij}\rangle = \frac{1}{\sqrt{T}}\sqrt{\int_0^T F_i^2(t)dt - 2\int_0^T F_i(t)c\sum_{i=1}^{N} I_{ij}\, F_i(t)dt + c^2\int_0^T\left(\sum_{i=1}^{N} I_{ij}F_i(t)\right)^2 dt} \tag{6-4}$$

The row signal $F_i(t)$ needs to be orthogonal, leading to

$$\frac{1}{\sqrt{T}}\sqrt{\int_0^T F_i(t)F_k(t)dt} = \begin{cases} F & for\ i = k \\ 0 & for\ i \neq k \end{cases} \tag{6-5}$$

For $c = 1/\sqrt{N}$ leading to

$$\frac{\langle U_{ij\ on}\rangle}{\langle U_{ij\ off}\rangle} = \sqrt{\frac{\sqrt{N}+1}{\sqrt{N}-1}} \qquad 6\text{-}6$$

And to $G_j(t)$ in Equation 6-3 as

$$G_j(t) = \frac{1}{\sqrt{N}} \sum_{i=1}^{N} I_{ij}\, F_i(t) \qquad 6\text{-}7$$

Equation 6-5 demonstrates that the law of Alt and Pleshko [43] also holds for the general row signals $V_{ri} = F_i(t)$, i = 1,2,…, N and the pertinent column signals $V_{cj}(t) = G_j(t)$, j = 1,2,…, M in Equation 6-7, where $F_i(t)$, I = 1,2,…, N are orthogonal.

For PM-OLED the pixel luminance is proportional to the OLED current and the duration of this current. In the multiline driving method of PM-OLED, the image matrix D is decomposed by a matrix with same values in two adjacent lines (two-line matrix) as well as a residue matrix S through a complicated algorithm. Thus, in the Consecutive Multiline Addressing (CMLA), the image D could be decomposed to:

$$D = M2 + S \qquad 6\text{-}8$$

M2 in equation 6-8 could be formulated as shown in 6-9:

$$M2 = \begin{pmatrix} M2_{11} & M2_{12} & \dots & M2_{1m} \\ M2_{11} & M2_{12} & \dots & M2_{1m} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} + \begin{pmatrix} 0 & 0 & 0 & 0 \\ M2_{21} & M2_{22} & \dots & M2_{2m} \\ M2_{21} & M2_{22} & \dots & M2_{2m} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} + \cdots + \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ M2_{n-1,1} & M2_{n-1,2} & \dots & M2_{n-1,m} \\ M2_{n-1,1} & M2_{n-1,2} & \dots & M2_{n-1,m} \end{pmatrix}$$

$$= \begin{pmatrix} M2_{11} & M2_{12} & \dots & M2_{1m} \\ M2_{11} + M2_{21} & M2_{12} + M2_{22} & \dots & M2_{1m} + M2_{2m} \\ \vdots & \vdots & \dots & \vdots \\ M2_{n-2,1} + M2_{n-1,1} & M2_{n-2,2} + M2_{n-1,2} & \dots & M2_{n-2,m} + M2_{n-1,m} \\ M2_{n-1,1} & M2_{n-1,2} & \dots & M2_{n-1,m} \end{pmatrix} \qquad 6\text{-}9$$

And the residual single line matrix S is shown in 6-10:

$$S = \begin{pmatrix} S_{11} & S_{12} & \dots & S_{1m} \\ S_{21} & S_{22} & \dots & S_{2m} \\ \vdots & \vdots & \vdots & \vdots \\ S_{n1} & S_{n2} & \dots & S_{nm} \end{pmatrix} \qquad 6\text{-}10$$

The values of the two-line matrix M2 could be controlled by a two-line addressing. [44] Since two pixels of a column may produce light at the same time, the OLED current amplitude may be halved. Due to the common physical characteristics of LCD and Ch-LCD, where is optical performance is controlled by RMS voltage value, the multiline driving method for conventional passive matrix LCD is to be applied for driving the cholesteric LCD.

6.2 Multiline Driving of the Conventional Ch-LCD Driving Scheme

With regards to the driving of the Ch-LCD, the multiline driving could differ from that in the PMLCD's driving. The dynamic driving scheme of the cholesteric needs firstly switch the pixels into the homeotropic state before the selecting stage. Therefore it could not be achieved by dividing the voltage amount to two parts.

Ch-LCD is a voltage driving display. The display pixels response to the voltage amount applied on it. In the conventional driving method, the row and column voltage fields are added to achieve the high and low voltage fields across the pixel. However, the multiline driving could be possible if we can generate all of the possibilities of the one-off combinations in the two lines. This has been proposed in SID 2011 by adopting a conventional driving method. [45]

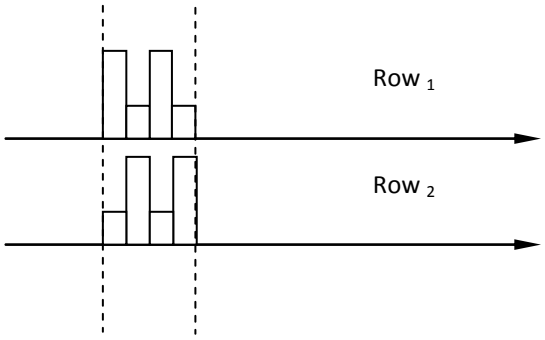


Fig. 6-2 Two different waveforms in adjacent rows

Figure 6-2 depicts the waveform pattern in adjacent rows of the conventional driving scheme. During each driving period, two rows are controlled simultaneously but by different signals. The driving scheme is to generate four different waveform types on the column lines and the waveforms in the adjacent two rows are always in the type depicted in Figure 6-3. After the driving starts, the overlapped waveforms could have one of the four different shapes as well as four RMS voltage fields' pair in the two adjacent lines as illustrated below.

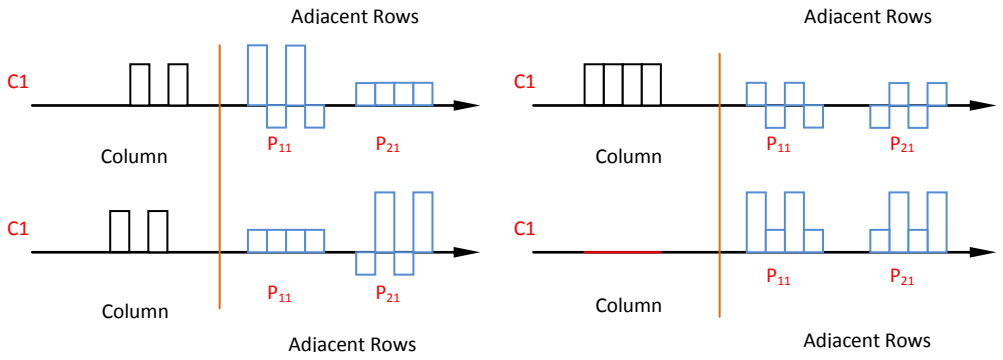


Fig. 6-3 Illustration of the two-line addressing under the conventional driving scheme

Figure 6-3 shows the waveforms details of the adjacent two rows and columns. As can be seen from the figure above, the waveforms in the column lines have four possible types as shown on the left side of c1. Each type of the column waveforms generates a different combination of on and off states pixel pair on the two adjacent rows as shown in the right of c1. So the overlapped waveforms have four various combinations during the two line selections which are S-NS, NS-S, NS-NS and S-S (S represents Select and NS represents No-Select).

That`s to say, by generating one of the four waveform types in the column lines, the adjacent two rows could achieve all of the possible combinations. Upper left stands for 1/0 (1 (Planer) for the first row and 0 (Focal Conic) for the second row), lower left for 0/1, upper right for 0/0 and lower right for 1/1. Thus, two rows could be controlled simultaneously so that the addressing time for a complete frame is halved.

However, the conventional driving method is too slow. It cannot compare with the dynamic driving method in terms of the driving speed even if it adopts the multiline driving method. The multiline driving in the dynamic driving scheme, if properly designed, could be useful to further increase the driving speed. In the next section, we will discuss the multiline driving in the dynamic driving scheme of the Ch-LCD.

6.3 Multiline Driving in the Enhanced Dynamic Driving Scheme

In the dynamic driving scheme, we also want to employ the multi line driving which will increase the driving speed largely as well as reducing the power consumption. In the dynamic driving scheme, the multiline driving could be applied by creating two types of driving waveforms in the selection stage of two rows and four types of waveforms in the column. Theoretically, if the overlapped voltage fields could cover all of the combination of bright and dark driving pairs, the

two line control is applicable. Based on this theory, we have designed the waveform pattern which could successfully drive the two adjacent rows.

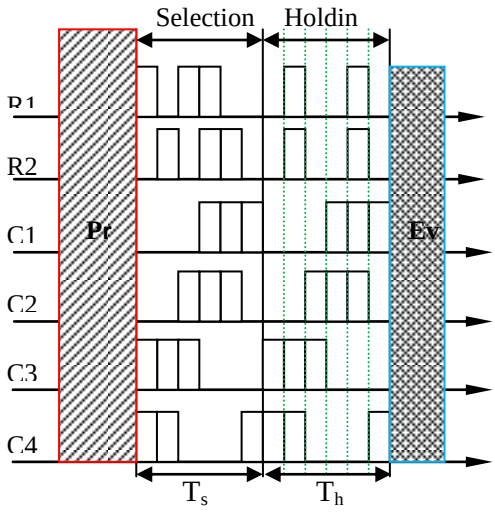


Fig. 6-4 Selection and holding waveforms for two adjacent rows

Figure 6-4 demonstrates the waveforms of the two rows addressing of the selection and holding stages in the enhanced dynamic driving scheme we have proposed in Chapter 3. In the selection stage, the row waveform has two possible types and the column has four. The holding waveform in all rows is the same and the overlapped voltage field in all holding stages must have a constant value for a stable holding.

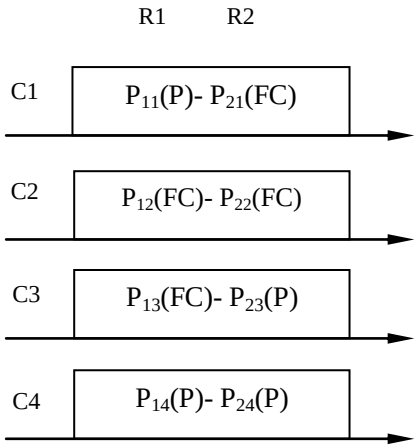


Fig. 6-5 Four switching combination in two adjacent rows

Figure 6-5 shows the selection result of row R1 and R2 when the column waveforms in four patterns are denoted by C1, C2, C3 and C4. By creating one of the four waveform types of the column lines, the two pixels of a row could have four different combinations of the planer pixel and focal conic pixel which could cover all of the possibilities.

In order to explain this method in details, in Figure 6-6 the cross pixel waveforms in the selection stage of two rows are drawn. From Figure 6-6 we could observe when the first row and the second row will get four types of combinations of 4/6 and 2/6 RMS voltage field. From the dynamic driving scheme described before we know that this would drive the pixel into planer and focal conic state at a six division waveform pattern.

It could also be noticed from Figure 6-6, the holding waveform will remains constantly at a value 3/6 of the applied voltage field so the holding part is constant and avoids any random fluctuation of the RMS values. Since it is a simple four stages dynamic driving scheme, the voltages used in this method are the same as those used in the enhanced DDS we addressed previously.

There are three voltages 48 V, 38 V and zero are used in the method. The driving speed could be doubled at about 0.5 milliseconds per line in average.

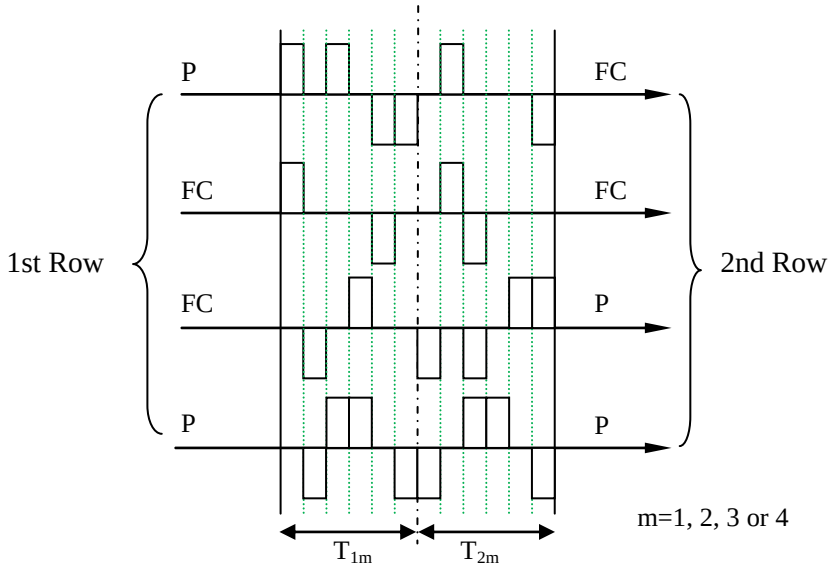


Fig. 6-6 The cross pixel waveforms in the selection part in four different combinations

The multiline driving method we are discussing here has is able to drive both the two adjacent rows and two discrete rows. Besides, three of more rows could also be controlled simultaneously what requires a more complicated driving waveform.

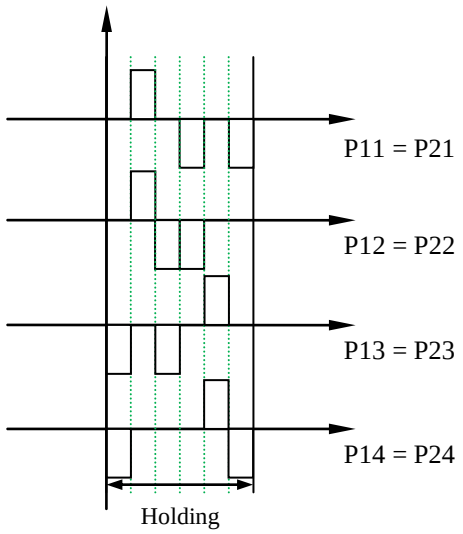


Fig. 6-7 the waveform in the holding part in four different combinations

To verify the proposed the driving method, we have adopted the method in a driving of a 40 lines Ch-LCD demo panel. The result is shown as below.

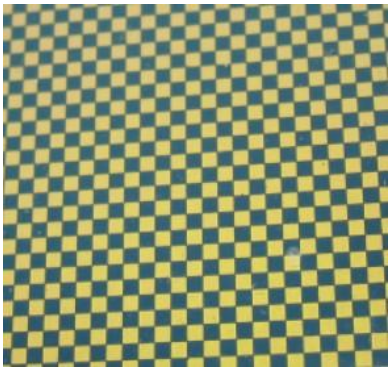


Fig. 6-8 Chess board created by multiline (two adjacent) addressing in the DDS of Ch-LCD

As can be seen from the photo in Figure 6-8, chess board image has been created by the proposed multiline driving on a demo cholesteric display panel. It cannot be distinguished which two adjacent rows are addressed simultaneously. The image is of same good quality compared to those created by the single line addressing dynamic diving scheme. The experiment has proven that the multiline method in the enhanced dynamic driving scheme is feasible.

6.4 Conclusion

The driving speed of the cholesteric LCD can be further improved even compared with the fastest dynamic driving scheme as previously discussed in Chapter 3. Similar with the multiline driving in the passive matrix display such as passive matrix LCD and PM-OLED, in the driving of the cholesteric LCD, the multiline driving is also possible. The multiline driving could further enhance the driving speed which is meaningful in the e-paper display's driving. The multiline addressing technology could also be implemented in our enhanced dynamic driving scheme. The driving speed is increased further for many folds. The result of our experiment shows that the multiline driving method in combination with the dynamic driving scheme could successfully further increase the driving speed and achieve the good image quality at the same time.

7 Driving Circuit Design

For visual validation, a specific discrete driver board has been designed to implement the diverse driving schemes for the Ch-LCD. Driving of the cholesteric LCD requires higher starting voltage to transit the initial states to the homeotropic state which is widely used in most of the fast driving schemes. There the driver circuit must be able to shift the control signal to the required high voltage level in order to trigger the shift of the states of the cholesteric texture. Besides, since several driving schemes which are proposed in the previous chapters need different driving conditions, the driver circuit should be designed to be flexible to execute all of the schemes. The Ch-LCD panel we used in experiments is a 160×160 square panel provided by the company AEG-MIS. In order to control this display, four independent driver boards are designed and manufactured to control the whole display panel. Each board also has the specially designed power supply to adopt different voltage group for different driving schemes. In this chapter we will discuss in details about the driver board design and its main devices in details.

7.1 Design Philosophy

The driver circuit is a vital component for testing and verifying of the driving schemes. Consider the cholesteric display panel we use is a 160×160 monochromatic Ch-LCD. The driver should have the ability to control at most 160 lines. Figure 7-1 shows the Ch-LCD we used for testing in the lab.

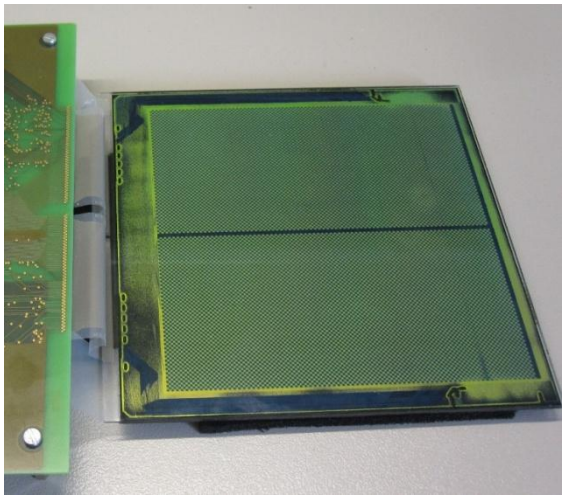


Fig. 7-1 Ch-LCD used in our experiments

As shown in Figure 7-1, the cholesteric LCD is connected to an interface board by two flexible cables on the left side. The interface board has eight plug-in interfaces installed on it. Each of the plug-in interfaces has 50 pins. 20 pins connect to the rows of the panel and 20 pins connect to the columns as well as 10 residual pins are connected to the ground. In this way the 160 lines are divided into 8 parts, each has the capacity to control a display area of 20×20 pixels. The eight parts are integrated to control the whole display. Any part of the display could also be controlled by one independent interface.

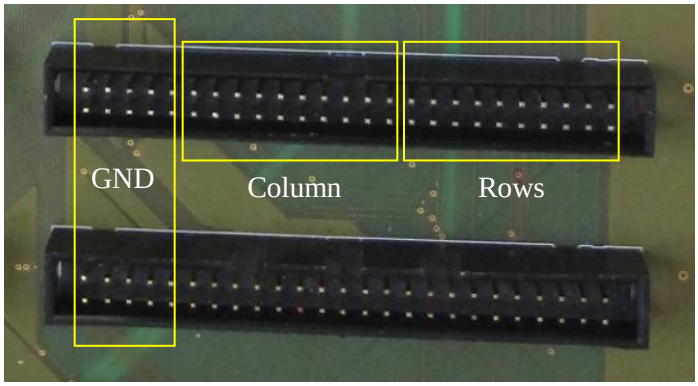


Fig. 7-2 Pins arrangement of the connectors of the interface board

Figure 7-2 depicts a part of the interface board with two plug-in interfaces. The pins arrangement of the interface could be observed in the figure above. Row and column pins could be easily controlled independently to adopt different driving methods with various voltage combinations. The control signal is generated by an FPGA. Signals are transferred and amplified through the driver board and external power supplies.

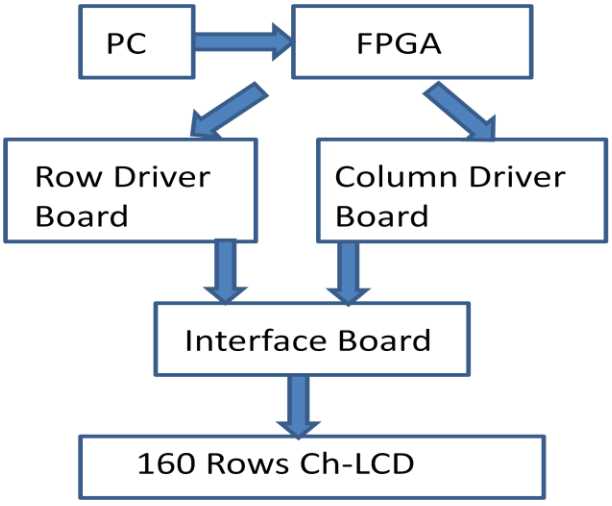


Fig. 7-3 Schematic diagram of the driver board and interface

Figure 7-3 shows the schematic diagram of the driver board and interface board to illustrate how the Ch-LCD panel will be controlled. In the PC side, the FPGA programming file, which was synthesized from a Verilog code, was downloaded to the FPGA board. The FPGA generated the row and column control signals by executing the programming code. PWM waveforms generated from the FPGA are then transferred to the row and column driver board. Since the driver boards need to test various driving schemes of the Ch-LCD, the row and column drivers are diverted in different boards to load various voltage groups. The PWM waveform will be amplified in the driver board through a level shifter circuit and outer power supplies. Finally, the waveform with the designed voltage amplitude was applied to the Ch-LCD panel through the interface board.

7.2 Driver Circuit Design

The design of the driver board needs to consider the connection first. Since the FPGA board we used has four identical output interfaces, the driver board was also divided into four boards with identical layout, but two of them are used for rows and two for columns.

The layout of the driver board can be seen in Figure 7-4.

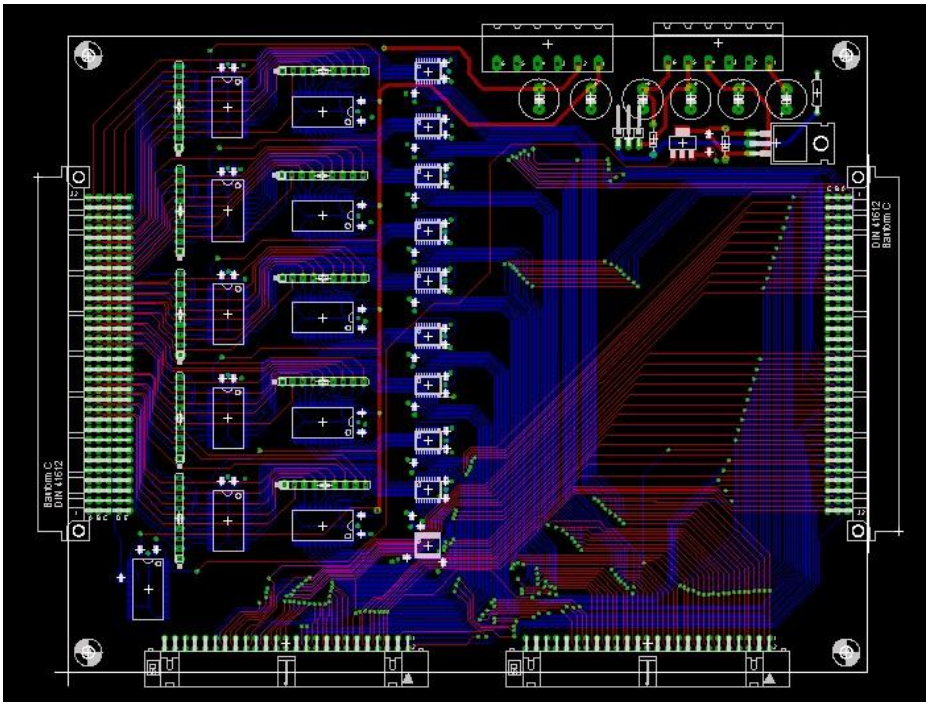


Fig. 7-4 Layout of the driver board

One of the four driver boards' layout could be observed in Figure 7-4. In the left side of the driver board is the interface to connect with the FPGA pins. The driving of the Ch-LCD requires high voltages, which in our experiments exceeded 40 volts. Thus the protection of the FPGA is important. In the left side of the driver board close to the connection pins, ten one-way buffers are used in between the FPGA and the level shifter ICs. These buffers could be destroyed if the high voltage is leaked to the circuit in the right side of the driver in case some problems happen. Thus, the expensive FPGA is protected in any unwanted errors.

The level shift IC in the driver board is used to shift the low voltage FPGA output signals to high voltage levels which are required in the driving of the Ch-LCD. To control the on-off of the high voltage levels to the level shifter ICs, there is a switch circuit and connection pins of the power supply located in the upper right side of the board as could be observed in Figure 7-4.

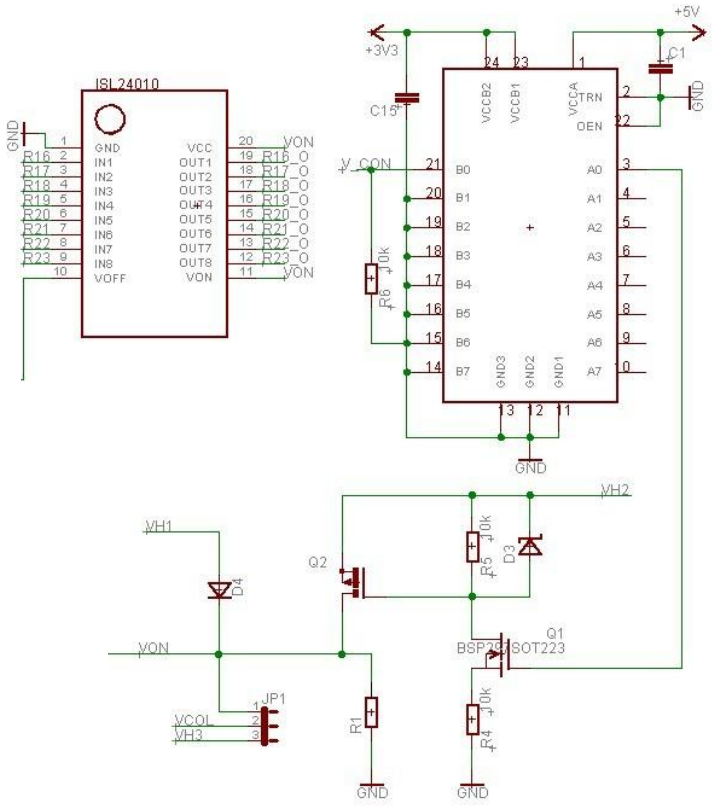


Fig. 7-5 Schematic of the switch on the driver board

Figure 7-5 shows the schematic view of the voltage switch part of the driver board. High voltage is applied at the gate and source end of the transistor Q2, The Q1 is the controlling transistor whose gate is connected to the FPGA output pins through a transceiver. The transceiver used here aims to protect the FPGA in case Q1 is defect. Control signals from FPGA will switch the Q1 to on and off state. When Q1 is switched on, voltage would be divided to R4, so the gate of the transistor Q2

would have the voltage value lower than the source side. Therefore the transistor Q2 would be turned on. High voltage VH2 would be added on the voltage pin of the level shifter chip. On the other side, if the transistor Q1 is turned off, because the voltage pin of the level shifter is always connected to the lower voltage VH1 through a diode, the lower voltage will be fed to the level shifter. Using this method, the low and high voltage could be controlled by the driving signal from the FPGA.

Two lower voltages 5v and 3.3v are used to control the transceiver IC in the driver board. Two positive higher voltages and a negative voltage were used to drive the cholesteric LCD. The arrangement of these voltage pins was shown as follows.

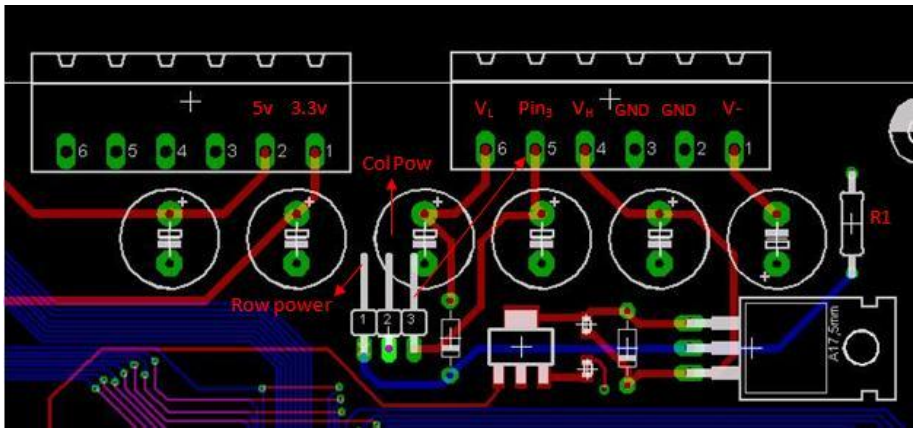


Fig. 7-6 Arrangement of the power supply pins

Figure 7-6 demonstrates the pin arrangement of the power supplies. The left side interface of the power supplies is to connect the one way buffer which requires 5v and 3.3v to work. The right side interface pins are used for level shifter. From Figure 7-6 we can observe that three voltage levels and ground pins are arranged in the interface. Higher voltages VL and VH are used in the whole scheme of the dynamic driving scheme. Instead of the zero volts, we use a V- here to achieve higher voltage level by overlapping with the positive levels.

7.3 Components Used In the Circuit

In this chapter the main components used in the driver board are listed. The list of the components used in the driver circuit is depicted in Table 7-1.

This table is the list of components used in making one of the four driver boards.

Name of device	Number per board	Value
ISL24010	10	
LVX4245	11	
BUZ272(PMOS)	1	
BSP297(NNOS)	1	
Diode	1	1n4007
Zener Diode	1	6V8
R1	1	3.3K
R2	1	1K
Jp1	1	
R-set	10	10k
MIRA Capacitor-SMD	53	100n
Capacitor	6	100n100v
Power interface	2	
FPGA Interface	1	160pin
Panel Interface	2	50pin
Backup Interface	1	96pin

Table 7-1 List of components used in the driver circuit

Two ICs are used in the driver circuit, one is the one-way buffer IC 74LVC4245A and the other is the level shifter IC ISL24010.

7.3.1 Transceiver IC

The transceiver IC used in the driver circuit is 74LVC4245A. This IC is an octal dual supply translating transceiver with three states.

INPUT		INPUT/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

Table 7-2 Function table of the 74LVC4245A

Table 7-2 shows the function table of the transceiver IC. On the driver board, the transceiver IC is used as a buffer between the high voltage circuit and the FPGA. As we have marked in the function table, in the driver circuit, we should give the OE and DIR low and high voltage levels respectively. In this function, when the input signal of the transiciver IC is 3.3V, the output will be 5V which is connected to the level shifter IC. Because of the one way conduction, the buffer could provide protection of the FPGA board and also output stable 5V pulses to the level shifter. [46]

The pin arrangeement of the transiever IC could be observed in Figure 7-7.

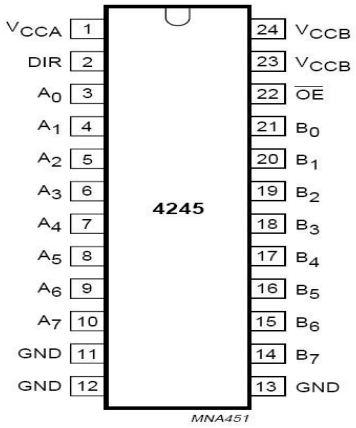


Fig. 7-7 Pin arrangement of the transceiver IC

It could be observed that the transceiver IC has eight input and output pins. Consequently, on one driver board, ten ICs are needed to buffer the 80 row and column pins and one IC is used to connect the switch control signal from the FPGA. The connection of the transceiver IC is shown in Figure 7-8.

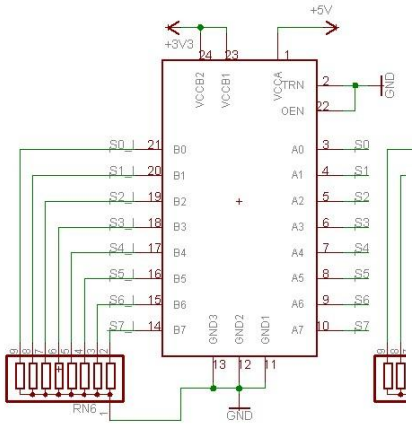


Fig. 7-8 Schematic of the connection

Because the output of the FPGA is 3.3 V, the lower voltage pin is connected to 3.3V and the higher output voltage pin is added on 5V to drive the next level shift. The resistor between the input pins and ground aims to keep the input at zero volts if no signals are applied.

7.3.2 Level shifter IC

Another important component in driver board is the level shifter IC. The level shifter IC we used in the driver circuit is called ISL24010 which is a typical octal voltage level shifter for TFT or LCD panels. Pin arrangement of the IC could be observed in Figure 7-8.

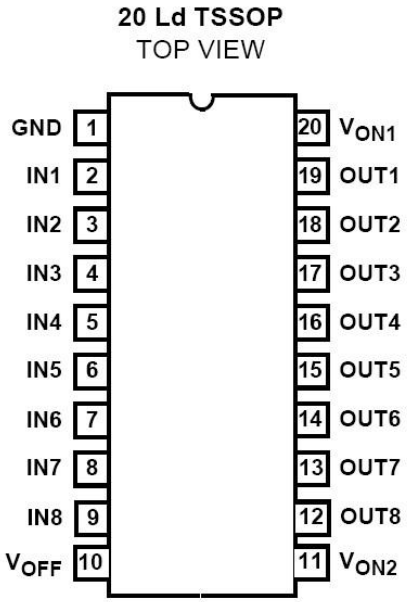


Fig. 7-8 Pin arrangement of ISL24010

Figure 7-8 shows the pin arrangement of the ISL”24010 which is contained in a TSSOP-20 pin package. This level shift could switch the input single to an output near or equal to its output supply voltages. There are the three voltage supplies in the IC. The Von1 and Von2 are the positive voltage pins and the Voff is the negative voltage pin. On the driver board, the Von1 and Von2 are connected together, so the eight input/output pins would have identical functions.

The positive voltage level may vary from 5v to 40v and the negative voltage level output varies from -20v to -5v. Thus the range of the Von to Voff lies between +10V and +60V which would be enough for the needed high voltage in the driving. The input voltage range varies in the range of -5V and +5V, and this could be guaranteed by the output of the transceiver IC. Because the transceiver IC has also eight output pins, 10 devices are needed in one driver board. [47]

7.4 Driver board

The completed driver boards together with all the connections and the FPGA board could be observed in Figure 7-9. Sockets on top of the driver board are used for testing. The output pins are located at the right side of the board. They are connected to the interface board through several cables.

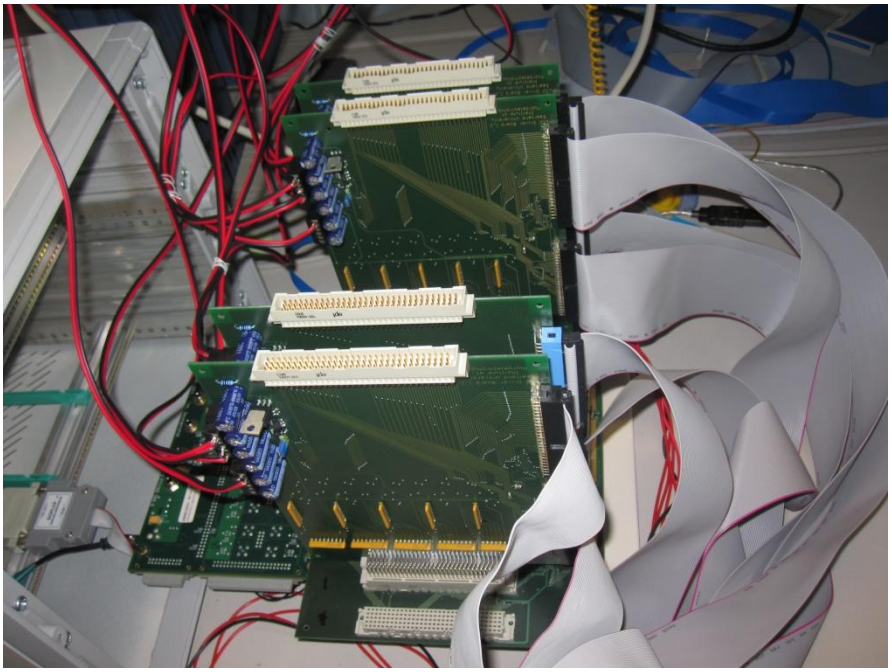


Fig. 7-9 Discrete driver boards with connections

7.5 Summary

In this chapter we designed and manufactured a discrete driver board set in the purpose of verifying the dynamic driving scheme and the gray scale's generation of the cholesteric LCD. The driver board with specially designed power supply circuit could adopt various voltage groups for various driving schemes. Because of the independent design of the driver board, display area from 40 rows to 160 rows could be controlled independently and it is easy to execute different driving schemes at different part of the panel. The design schematic and the layout view of the driver board are also given in this chapter as well as the critical devices used in the design. Good results were achieved by using this driver board which proven it fully meet the requirements of the design and the reliability is also quite good.

8 FPGA Implementation and Measurement

8.1 Introduction

Several driving schemes for binary and gray scale's driving have been proposed in details in the previous chapters. In this chapter we discuss the image processing and the FPGA coding for verification of these driving schemes. In the field of digital circuit design, the Verilog HDL is used to program the driving waveform generation using a FPGA. Various programs for dynamic driving scheme and the state of the art fast static driving scheme for multiple gray scales have been coded and executed. The results show good image quality and high driving speed in all driving method we used. Besides, the reflectance and the gray scales have been measured by the reflectance measurement set produced in our lab.

8.2 Image Processing by MatLab

To generate an image on the display panel, what we should do first is to adopt the image data into the pixel matrix. In every pixel dot, it will be a digital value to represent the voltage or current amount which will be applied on the pixel from the driver circuit. In order to generate a test image on the Ch-LCD panel by adopting the proposed dynamic driving scheme, the MATLAB tools are used for the image conversion. The M coding is listed below in Figure 8-1.

```
% input a image file
[filename pathname]=uigetfile('*.jpg;*.bmp;*png','choose
str=[pathname filename];
a=imread(str);
[x,y,z] = size(a)
for i=1:x
for j=1:y
%for k=1:z
b(i,j) = (sum(a(i,j,:))/3);
end
end
threshold =100;
c = double(zeros(x,y));
for i=1:x
for j=1:y
if b(i,j) > threshold
c(i,j) = 1.0;
else
c(i,j) = 0.0;
end
end
end
```

Fig. 8-1 Matlab code for image processing

The aim of the program is to convert an image into a binary-valued matrix to be used in the dynamic driving scheme. The cholesteric LCD we used is a single color LCD, thus the pixel matrix will include 1 or 0 at every pixel dot.

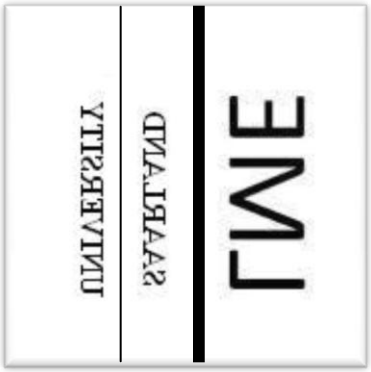


Fig. 8-2 Image used in the dynamic driving scheme

Figure 8-2 shows an image for testing of the enhanced dynamic driving scheme. The image is mirrored to the right to match the row and column's arrangements of the display panel. In the MATLAB, program will discrete the image into a 160×160 pixel matrix and each dot takes the value 1 or 0. Color image would also be switched to a binary-valued image since the display we used in test is monochromatic.

8.3 Verilog Coding and Results

Verilog HDL is used to design the driving waveform and to control the FPGA's output. Xilinx ISE is chosen as the programming and synthesis tool in experiments. The program consists of two parts. One of them is the code for two-value dynamic driving scheme. The other is the code for the gray scale's generation.

8.3.1 Binary-Value Coding

In the first place, the binary image processed by MATLAB will be generated in the cholesteric LCD by using the proposed dynamic driving scheme. As we have discussed before, the on and off of the pixel in the dynamic driving scheme are determined by the high and low voltages at the selection stage. As for the binary-value image, there are only two possibilities at the selection stage

which are 1 and 0. As a result, two types of waveform at the selection stage could be generated by checking the value of the pixel when driving.

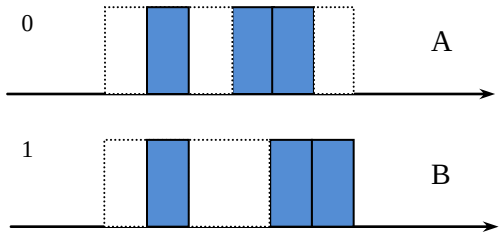


Fig. 8-3 Waveform in the column selection stage when loading 1 and 0

Figure 8-3 shows the waveform pattern generated by Verilog code. During the generation of the output waveform for driving, in each pixel, the program checks the value of the pixel. If it appears to be 0, the FPGA outputs the waveform pattern A. Otherwise, if the value is 1, waveform pattern B would be the outputted. In the display panel, the image will be driven row by row to the end.

Result could be observed in Figure 8-4.

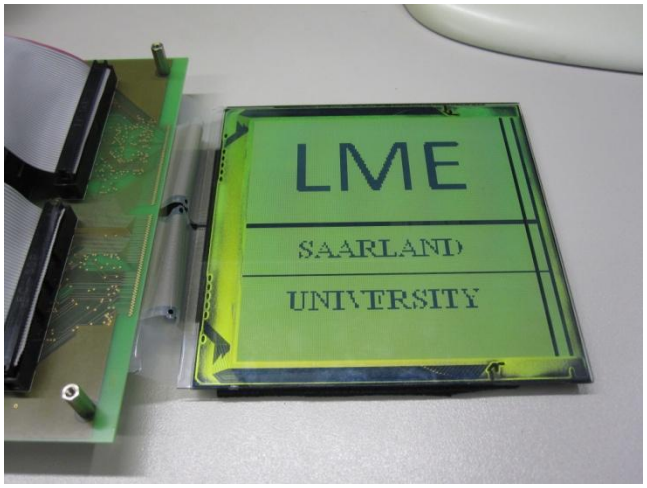


Fig. 8-4 Image generated by using the dynamic driving scheme

The image on the cholesteric LCD shown in Figure 8-4 is generated by the proposed enhanced dynamic driving scheme. It revealed that the dynamic driving scheme appears to work properly in controlling the display panel up to 160 rows. Moreover, it could also be observed that the contrast ratio appears quite high.

8.3.2 Gray Scale Coding

The gray scale's driving is more complicated than the binary-value driving. Within the gray scale's driving, the column waveform should be divided into many divisions to generate various gray scales. Gray scale is determined by RMS voltage field in the selection part in a small transition region, thus the division should be appropriately controlled.

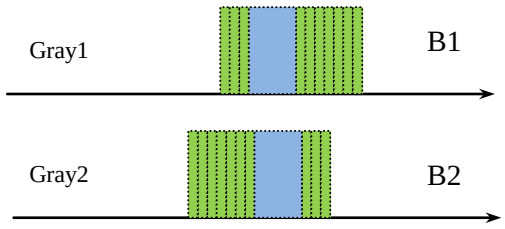


Fig. 8-5 Waveform at the column selection stage in gray scale's driving

Figure 8-5 shows the waveform pattern generated at the selection stage of the proposed dynamic driving scheme for gray scales. In the test of the gray scale's generation in a 40×40 display area, ten gray scales were expected to be achieved. By calculating the RMS values of the RV curve which has been done previously, we could get a look-up table including the gray scale and its waveform positions. In order to precisely control the RMS voltage value at the selection stage, the waveform was generated on both sides of the fourth division of the column lines as shown in Figure 8-5. The right side of the gray scale's green division removes one, the left side will be added one. Each movement matched a new gray scale because of the shift of the RMS values across the pixel.

By dividing the waveform into10 parts, the gray scale generated by the dynamic driving scheme could be observed in Figure 8-6.

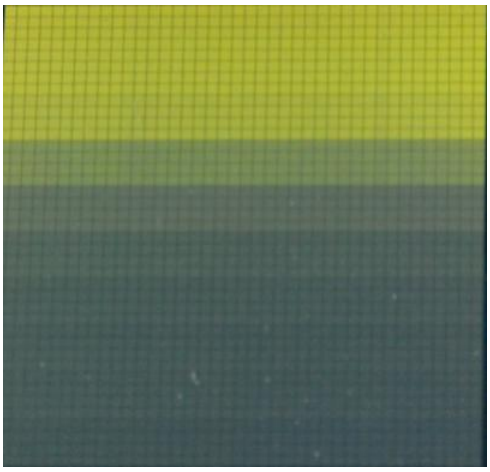


Fig. 8-6 Gray scale driving result

The Verilog code of the other part is identical to that in the binary-value dynamic driving scheme. In the new fast static driving scheme for more gray scales, the gray scales were generated by the same method.

8.4 Reflectance Measurement

The measurement of the reflectance is important for evaluating the contrast ratio and gray scale numbers of the reflective display. However, the reflectance's measurement is not so simple comparing to the measurement of the light emitting displays.

Emitting display such as OLED and LCD could be measured directly by the photo sensor in the dark environment. In respect to the measurement of the reflective display, there has to be an ambient light source to generate the light on the display's surface. The light source usually is strong comparing to the reflected light. Thus the primary question is how to measure the reflected light without being affected by the light emitted directly from the light source. The second challenge is to fully receive the reflected light.

A common solution for the questions we talked above is illustrated in Figure 8-7. As it could be observed in (a) of the Figure 8-7, when the light source emits light on the display surface vertically, the reflected light will be scattered in all directions, making it difficult to conduct the measurement. However, on the other side, as described in (b) of Figure 8-7, the reflected light will toward a vertical direction if the light source is around the display surface.

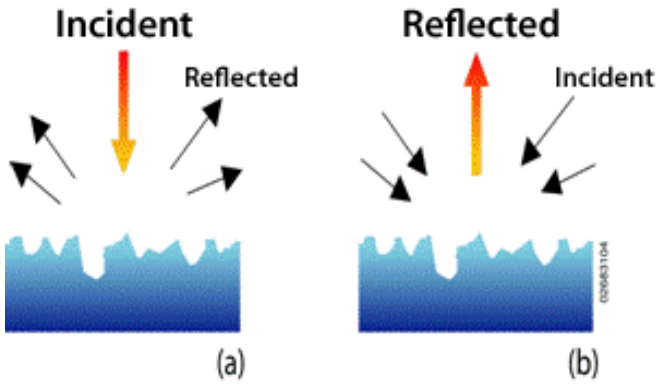


Fig. 8-7 Theory of the reflectance measurement

The cholesteric LCD is also a reflective display without any light emitting module. Thus the reflectance measurement should obey the rules as we discussed in Figure 8-7.

Figure 8-8 shows a special designed light source in the measurement set. As could be observed in Figure 8-8, the light source is in a circle shape inside the top of the dark chamber. The circle shape light source was located directly on the top of the display area which is under test. In the middle of the light source these is a hole, thus the reflected light could pass through. We can therefore obtain a high degree of reflectivity, by maximizing the amount of light reflected back.

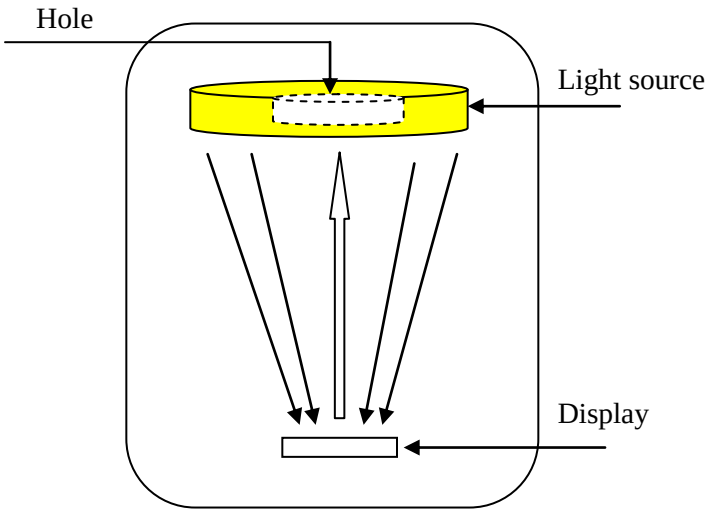


Fig. 8-8 Light source of the measurement set

Figure 8-9 shows the measurement set which targets at measuring the reflectivity and gray scales of the cholesteric LCD. The principle of the measurement set is based on the theory we have discussed in Figure 8-7.

Fig. 8-9 Reflectance measurement set

The measurement set is made up by three main parts. The first part involves a dark chamber with a cycle light source inside the top of it. On top of the dark chamber, a photo diode is installed to receive the reflected light from the test area of the display. A pico-meter was connected to the photo diode to read out the photo current value. The reflectance measurement set has been used for the R-V curve test of the cholesteric LCD, which is used in the determination of the key parameters for driving schemes. It has also been used for the gray scale's test. The results from both tests are used to calibrate the driving conditions.

8.5 Summary

In this chapter we have described how to generate the image on the cholesteric LCD. Image processing tools in MATLAB were used to convert the image into the pixel matrix which is used as the driving data for the control program. Verilog HDL is used as the programming language to control the FPGA for driving waveform's generation. The waveform arrangement and the correspondent results were also provided in this chapter. Last but not least, the reflectance measurement set had been developed and made in our lab to measure the R-V characteristics and the gray scales of the test Ch-LCD.

9 Conclusion

For a long time, the lack of effective driving scheme was a primary obstacle in the practicability of the Cholesteric LCD. Many driving schemes have been proposed in recent years such as conventional static driving scheme as well as several fast dynamic driving schemes (DDS). These driving schemes which are introduced in Chapter 3 features either good image quality or fast driving speed. As an improvement, we proposed the enhanced dynamic driving scheme with the ability to drive the Ch-LCD not only into the on-off state but also several distinct gray scales. In the enhanced dynamic driving scheme, the selection and holding waveforms are newly designed to ensure pixels could be driven to certain reflectance while the unselected pixels would not be affected. Different from the five voltages used in the U/$\sqrt{\frac{3}{2}}$ DDS, only three voltages are needed in the new enhanced dynamic driving scheme. The highest driving voltage was also reduced by 12% comparing with the U/$\sqrt{2}$ DDS. Driving speed is 1.2 ms / line which is higher than many dynamic driving schemes. So this enhanced DDS scheme shows in nearly every aspect better performance and better parameters.

Gray scale is possible in the bi-stable Ch-LCD and actually a mixture state of the reflective planer state and the scattering focal conic state. In the enhance DDS proposed in Chapter 3, gray scales are created in the Ch-LCD by using root of mean square (RMS) value of the applied voltage instead of modulating voltage levels. Thus, gray scales could be created by different RMS voltage values which are achieved by shifting the duty cycle of driving waveforms. The number of voltage sources could be reduced so that the complexity and the cost of the driver may be significantly reduced.

Due to the intrinsic characteristics of the Ch-LCD that the state transition is quite steep in the DDS, the gray scale number generated by this method is rather modest. In order to increase the gray scale number in the enhanced DDS, we have proposed a new method named Multi-Selection method (MSM). This method is to scan the display two or more times during the driving. Thus, the gray scales could be generated in two or more steps which could at least make the gray scale number doubled without increasing hardware cost. The gray scales in the dark side are also extended which meets the nonlinear requirement of the gamma correction. During the experiments, two- and three-selection methods were executed in the gray scale's driving. Considering that the three- or even four-selection method consumes more time but increase the gray scale number only a little bit compared with the two-selections method, the two-selection method is recommended.

In the gray scale's driving of the Ch-LCD, the uniformity of the generated gray scales is another issue of concern. Unfortunately, the uniformity of the gray scale generated by the DDS is not satisfactory no matter in the one-selection or multi-selection method. In order to improve the gray

scale's uniformity in a fast driving speed, we proposed a fast static driving scheme based on the state transition from one stable state to another stable state but not via a meta-stable state. The generated gray scales show good uniformity compared with the gray scales generated by the DDS. Because the state transition happens at the left side of the R-V curve which is smoother than the right side, the gray scale number is also increased. However, the fast static driving is roughly two-times slower than the enhanced DDS.

A further method to increase the driving speed is the multiline driving method which is proven for PM-LCD and PM-OLED. Two-line addressing waveforms have been designed in the enhanced dynamic driving scheme to achieve four combinations of the driven state. In experiments and tests on Ch-LCD panel, good result has been achieved. The multiline driving method for the Ch-LCD could reduce nearly 50% of the driving time which is especially meaningful for large high resolution displays.

In order to validate the diving schemes proposed in this thesis, four discrete driver boards have been designed and manufactured. All of the proposed driving schemes have been executed on a 160×160 Ch-LCD (Provided by AEG MIS) through the driver board. A Vertex 5 FPGA was used as the signal generator. Experiment results showed very good consistency with the design objectives. This has proven that the new driving schemes proposed in this thesis are correct and effective.

Due to the synergy with the mainstream LCD technology and other technical amenities, cholesteric LCD is a promising candidate for the next generation's color e-paper display. The higher driving speed, higher gray scale resolution, better uniformity and simple driver architecture may strengthen a little the competitiveness of Ch-LCD. In combination with potential improvements in other characteristics like reflectance and color reproduction etc, the Ch-LCD may become a wide-spread e-paper technology.

10 Appendix

EPD: Electronic Paper Display

LCD: Liquid Crystal Display

OLED: Organic Light Emitting Diode

CRT: Cathode Ray Tube

QR-LPD: Quick Response- Liquid Powder Display

EWD: Electrowetting Display

R2R: Roll to Roll

Ch-LCD: Cholesteric Liquid Crystal Display

EFD: Electrofluidic Display

ECD: Electrochromic Display

ITO: Indium Tin Oxide

IMOD: Interferometric Modulator Display

UV: Ultraviolet ray

HTP: Helical Twisting Power

DDS: Dynamic Driving Scheme

P: Planer state

FC: Focal Conic state

Homo: Homeotropic state

P*: Transient Planer state

PSCT: Polymer Stabilized Cholesteric Texture

SSCT: Surface Stabilized Cholesteric Texture

θ: Angle of incidence

λ: Wavelength of the incident light

$\bar{n}$: Average refractive index

P_0: Pitch of the cholesteric texture

$\Delta\lambda$: Width of the reflection band

K_{22}: Twist elastic constant

ε: Dielectric anisotropy

RMS: Root of Mean Square

Ts: Selection time of the dynamic driving scheme

Γ: Transition time from the Homo to P^*

Up-ev: Voltage of the pre-selection stage

Ucol: Voltage of the column line

FPGA: Field Programmable Gate Array

PHM: Pulse Height Modulation

PWM: Pulse Width Modulation

MSM: Multi Selection Method

x: The concentration of the dopant

LS: Light source

BL: Back light

GS: Gray Scale

R-V: Reflectance – Voltage

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