A 120 GS/s 2:1 Analog Multiplexer with High Linearity in SiGe-BiCMOS Technology

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***Abstract*—A 2:1 analog multiplexer (AMUX) in SiGe BiCMOS technology with a record sampling rate for SiGe-technology of 120 GS/s, is presented. The AMUX is intended to double the signal bandwidth of two 8-bit digital-to-analog-converters and achieves an effective resolution (ENoB) of 7.7 bit, at low frequencies as well as 5.1 bit at 48.8 GHz and 4.1 bit at 58.6 GHz for sampling rates of 100 GS/s and 120 GS/s, respectively. These are the highest resolutions reported for an AMUX in any kind of semiconductor technology. The results were obtained by a simple selector-circuit concept that was carefully optimized in the frequency domain with regard to balanced signal paths. The AMUX performance was demonstrated by measurements on an RF-module bondwire-assembly of the AMUX-chip.**

I. Introduction

In the recent years, analog multiplexers (AMUX) as introduced in [1] became popular as they can double [1]–[4] or quadruple [5] the output signal bandwidth and the sampling rate of digital-to-analog-converters (DAC) by time-interleaving. Currently, the main application area of AMUXs is to increase the transmission capacity per bandwidth in optical communication systems [2], [3]. The highest generated symbol rate of $168\,\mathrm{GBd}$ for a PAM-4 signal is demonstrated in [2] for a 2:1 AMUX in a $250\,\mathrm{nm}$ InP DHBT technology with $f_T/f_{max} = 460\,\mathrm{GHz}/480\,\mathrm{GHz}$, however, no numbers on linearity are presented. In a $55\,\mathrm{nm}$ SiGe-BiCMOS technology, the 4:1 AMUX in [5] can generate PAM-4 signals at a maximum symbol rate of $100\,\mathrm{GBd}$ with a circuit concept that is based on generation and summation of return-to-zero signals from input signals. The linearity of this circuit, characterized by the ENoB, ranges between $4.9\,\mathrm{bit}$ at $3\,\mathrm{GHz}$ and $4.2\,\mathrm{bit}$ at $40\,\mathrm{GHz}$. A comparatively simple analog selector circuit concept in a SiGe-BiCMOS technology with $f_T/f_{max} = 300\,\mathrm{GHz}/500\,\mathrm{GHz}$ achieves a maximum PAM-4 signal symbol rate of $56\,\mathrm{GBd}$ [4]. The AMUX reported in this paper applies the same circuit concept but operates up to a PAM-4 symbol rate of $120\,\mathrm{GBd}$, which is the highest symbol rate reported for an AMUX in SiGe-bipolar technology. Furthermore, the ENoB at $120\,\mathrm{GS/s}$ ranges between $7.7\,\mathrm{bit}$ at $270\,\mathrm{MHz}$ and $4.1\,\mathrm{bit}$ at $58.6\,\mathrm{GHz}$, which is the highest linearity over such a frequency range reported for an AMUX in any kind of semiconductor technology. The circuit is realized in the scope of the European Horizon 2020 program TARANTO and is co-funded by the German BMBF (grant agreement No. 737454), with the aim to explore the performance limits of an AMUX for signal bandwidth extension of 8-bit DACs beyond $50\,\mathrm{GHz}$. The AMUX circuit concept is briefly described in section II. Section III introduces linearity design considerations in the frequency domain, which are applied in section IV to explain the effect of clock related linearity impairments in a comparison between designs for 6- and 8-bit resolution. Measurement results of the AMUX in an RF-module assembly are shown in section V.

II. AMUX Circuit Concept

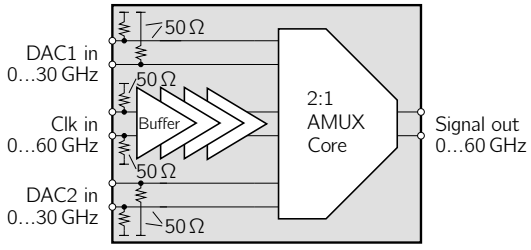

Fig. 1: Block diagramm of the 2:1 AMUX IC.

Fig. 1 shows the block diagram of the differentially operated AMUX, that was designed based on the cell based methodology in [6] with a topology suggested in [4]. The circuit consists of a core cell shown in Fig. 2, with two linear transadmittance stages (TAS1,2) at the signal input, which are driven by the output signals of the two external DACs (DAC1,2), whose bandwidth shall be doubled by the AMUX. The differential output currents of TAS1,2 (i.e. the DAC1,2 signals) are fed into the emitter-nodes of a selector stage (SEL). The SEL commutates, alternating with the clock polarity, each differential signal current either via a common-base-stage (CBS) to the AMUX output or via a dummy CBS (not shown in Fig. 2) to ground. This operation can be modeled by a multiplication of each of the differential SEL input currents with a 10- or an inverted 01-sequence depending on the respective clock phase. The function of the CBS at the output is based on its low input impedance. It sums up both differential signal currents and it improves the isolation between SEL output and the clock input. Thereby, it reduces intermodulation products in the AMUX output spectrum. The input clock of the clock path is amplified by four differentially operated buffer cells with a total voltage gain of 20, each consisting of a load resistor pair followed by

two emitter follower pairs (EF), a current switch (CS) and a CBS. Furthermore, access ports for offset measurement and cancellation were implemented at the in- and output of the final clock buffer stage.

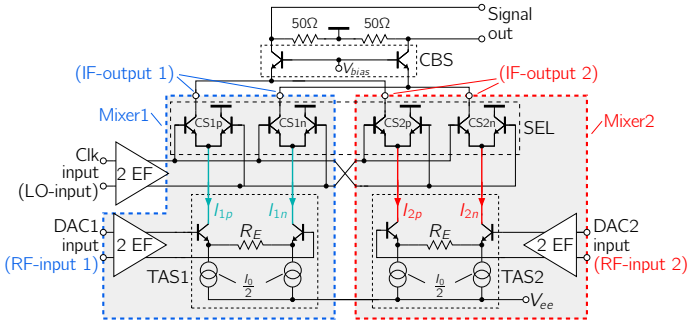

Fig. 2: Circuit principle of the 2:1 AMUX core.

III. AMUX Linearity Considerations

The linearity in terms of the ENoB $= (\text{SINAD} - 1.76)/6.02$ depends on the signal-to-noise-and-distortion ratio (SINAD) of the AMUX output spectrum, which is evaluated up to twice the DAC1,2 Nyquist bandwidth (i.e. up to f_{clk}). It is therefore advisable to create an explanatory model for the AMUX linearity in the frequency domain. The 10-/01-multiplication of the DAC1,2 signals by the SEL, as described in section II, can be modeled by an unbalanced mixer in each differential signal path [3] (cf. Fig. 2). The LO-inputs of the mixers are driven by a clock frequency f_{clk} that equals the sampling rate of DAC1,2. The RF-inputs are driven by the respective DAC1,2 signals, which are shown in the left column of Fig. 3 by their sinc-envelope in the 1st and 2nd Nyquist bands. Higher Nyquist bands are not shown as their contribution to the ENoB is comparatively small. DAC2 is operated at the inverted (180° phase-shifted) DAC1 clock (cf. Fig. 7), thus the signal phases in the DAC2 2nd Nyquist band are likewise inverted. This is indicated in Fig. 3 by flipping the inverted content upside down to the lower half plane.

These DAC1,2 spectra at the RF inputs represent the base-bands that appear at the IF outputs of the unbalanced mixers with their amplitudes scaled by the mean (ideally 0.5) of the respective 10-/01-clock-sequence. In addition to these spectra the main contributor to the spectrum at the IF-output of the mixers are their mirrored upconverted images in the sideband below f_{clk}, shown in the right column of Fig. 3. As Mixer2 in the DAC2 path is operated at the inverted Mixer1 clock (cf. Fig. 2), the signal phases of the mirrored DAC2 image are likewise inverted. Finally, the IF output of both mixers is summed up by the CBS at the AMUX output. Thus, the spectrum at the AMUX output is given by a superposition of all spectra shown in Fig. 3. The resulting frequency band up to the DAC1,2 Nyquist frequency f_n represents the targeted lower band and the DAC1,2 second Nyquist band up to f_{clk} represents the upper band of the targeted AMUX output spectrum, which has thereby twice the bandwidth of the original first Nyquist bands of DAC1,2.

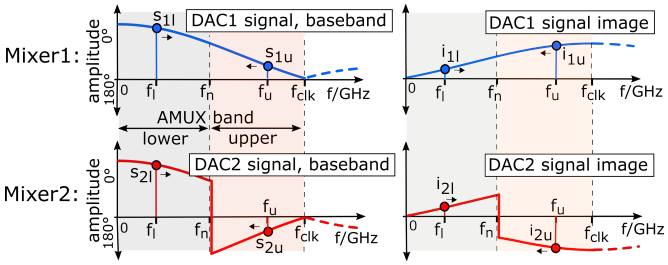

Fig. 3: Spectra at the IF outputs of the SEL mixer-models.

The creation of a single tone is of interest as the SINAD of the related spectrum is evaluated for the AMUX linearity in terms of the ENoB. Fig. 3 shows the creation of a tone at a frequency f_l in the lower AMUX band. DAC1,2 create this tone with equal amplitude and phase, which also appears at $f_u = f_{clk} - f_l$ in the second Nyquist bands of DAC1,2 but at inverted phases due to the DAC2 clock inversion. The superposition of these DAC1,2 baseband signals (left column of Fig. 3) and their mirrored upconverted image (right column of Fig. 3) constitute the final output spectrum. Therein the tones at the target frequency constructively (i.e. $s_{1l} = s_{2l}$, $i_{1l} = i_{2l}$) sum up to the final amplitude while the tones at f_u cancel each other out due to their inverted phases (i.e. $s_{1u} = -s_{2u}$, $i_{1u} = -i_{2u}$). A tone at a frequency f_u in the upper AMUX band is correspondingly created (not shown in Fig. 3) if the phase of the DAC2 tone at f_l in the previous example is inverted, which inverts all phases in the Mixer2 row in Fig. 3. In this case it is $s_{1l} = -s_{2l}$, $i_{1l} = -i_{2l}$ whereby the tone at f_l cancels out while the tone at f_u is sustained due to $s_{1u} = s_{2u}$, $i_{1u} = i_{2u}$.

The ideal cancellation of the unwanted tones depends on equal signal amplitudes and an ideal clock phase inversion of 180°, which requires to balance both signal paths from the DAC1,2 outputs up to the superposing CBS. Any residues of unwanted tones due to an imbalance degrades the SINAD and thereby the ENoB. In contrast to imbalances in the signal transfer characteristics from the DAC1,2 outputs to the SEL, there are imbalances in the clock signal at the SEL, that turned out to be the major source for linearity degradation in this design and shall therefore be discussed in the following section.

IV. Clock-Related Linearity Impairments

A. Clock Offset and Duty Cycle Error

As explained in [7], a clock buffer chain as employed in the AMUX can show at its output a strong rise of duty-cycle error and related clock dc offset in a certain frequency range close to the intended operating frequency. At maximum clock frequencies in the $50 - 60\,\text{GHz}$ range, this offset was measured to be about $100...120\,\text{mV}$. In the linear region of the clock-buffer transfer functions this offset can be modeled by an effective clock-input related offset of $5...6\,\text{mV}$, which ranges between the 4 and $8\,\text{mV}$ offset curves in Fig. 4a. The ENoB traces shown are simulated at $100\,\text{GS/s}$ and $600\,\text{mVpp}$ differential clock input voltage-swing for ideal DAC1,2 signals

with 6- and 8-bit resolution. In comparison with no clock offset, the ENoB of a 6-bit input signal degrades over a 50 GHz frequency range by only 0.6 bit (11%) while an 8-bit input signal loses 1.7 bit (25%). This result points out the importance of clock dc offset cancellation, especially as in the presented design an 8-bit resolution and a high signal bandwidth is aimed at.

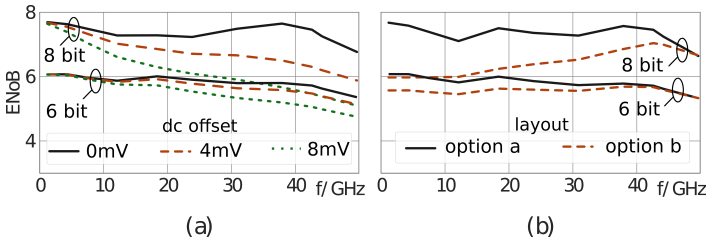

Fig. 4: Impact of (a) a dc clock offset and (b) of the SEL layout on the simulated ENoB at the 100 GS/s, for ideal DAC1,2 signals with 6- and 8-bit resolution.

The root cause of the observed ENoB degradation over frequency becomes visible by hand of the explanatory model in section III for the example of a tone created at f_l shown in Fig. 3. Any offset in the clock path leads to duty-cycle distortion of the 10-/01-sequence at the LO-port of the unbalanced-mixer model. As the two mixers operate at inverted 10-sequences, a duty-cycle distortion results in a positive and a negative deviation from the ideal sequence-mean. The DAC1,2 signals (i.e. the basebands) at the mixers' RF inputs are scaled by these unequal means and appear with unequal amplitudes at the IF outputs and thus the unwanted tone at f_u in the basebands is not ideally canceled out ($s_{1u}+s_{2u} \neq 0$) in the final superposition. The resulting residue reduces the SINAD and thereby the ENoB. For increasing frequency of a created tone f_l the frequency f_u of the unwanted tone decreases (cf. Fig. 3) and thereby moves along rising amplitudes of the sinc-envelope. The imbalance between these rising amplitudes leads to rising residues over frequency and represents the root cause of the decreasing AMUX linearity over frequency.

B. Layout related clock delay

An opposite characteristic, where the ENoB improves over frequency, can be observed in the presence of imbalanced delay between the CSs in the SEL-stage. Fig. 5 shows two options of the SEL layout with the driving final EF-transistor (EF2) of the clock path (cf. Fig. 2). Fig. 4b shows the impact of the two layout options on the ENoB of the AMUX in comparison between ideal 6- and 8-bit DAC1,2 input signals. At low frequencies, compared to option (a), option (b) degrades the ENoB by 0.5 bit (8%) at 6-bit DAC1,2 resolution and by 1.7 bit (22%) at 8-bit resolution.
The result shows that, despite the attempt to equalize interconnect lengths in layout option (b), option (a) is the better choice in terms of linearity. The reason is due to the distributed interconnect resistance that is shown in Fig. 5 in the form of a simple resistor-model. An interconnect section of option

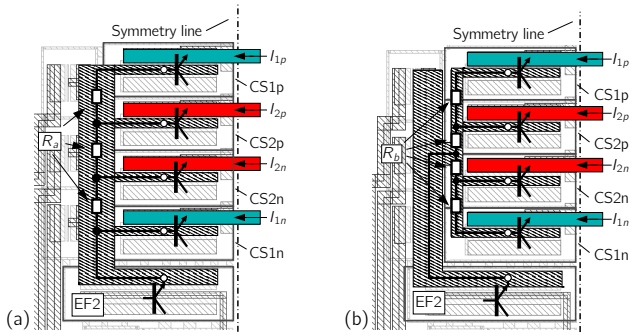

Fig. 5: Layout options to connect the SEL CS-transistors to the driving EF2. Only one half of the symmetrical layout is shown.

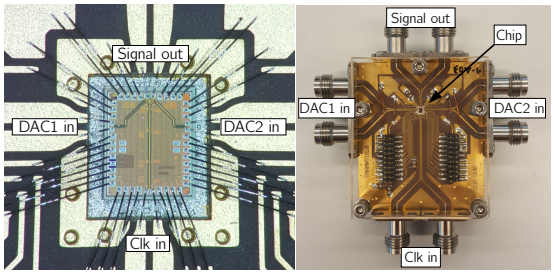

Fig. 6: AMUX IC bondwire assembly (a) and RF-module (b).

(a) has $R_a \approx 1.5\,\Omega$, while for option (b) $R_b \approx 3\,\Omega$ is larger due to the smaller widths of the metal stripes. These resistances together with the base-emitter capacitances of the transistors cause a distributed RC-link (parasitic inductance is negligible) that introduces clock delays between the CSs. Layout option (a) causes in the DAC1 signal path clock delays of 900 fs and 0 fs at CS1p and CS1n, respectively, as well as in the DAC2 signal path 600 fs and 300 fs at CS2p and CS2n, respectively. Simulations show that these different delays in each signal path average out to about the same delay for the clock in both signal paths which preserves the ideal 180° phase inversion between both mixer clocks. In contrast, layout option (b) introduces a 600 fs delay between the CS-pairs CS1p/n and CS2p/n of both signal paths, whereby the ideal 180° phase shift is changed by 6%. This phase does not alter the baseband amplitudes in the left column in Fig. 3 but it leads to imbalanced 0°/180° amplitude pairs of the unwanted tone at f_u in the DAC1,2 signal images in the right column of Fig. 3. These amplitudes follow the mirrored sinc-envelope and thereby decrease with increasing frequency. The related residues of the imperfect cancellation decrease accordingly towards zero, which explains why the linearity of layout option (b) in Fig. 4 recovers over frequency and finally approaches the ideal 180°-result of option a) at the clock frequency f_{clk}.

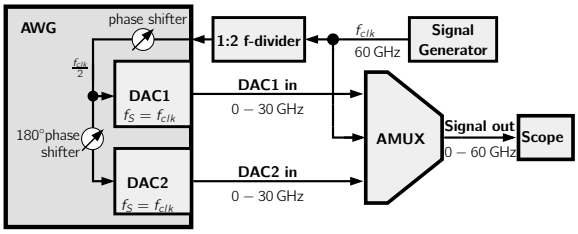

Fig. 7: AMUX measurement setup.

V. Measurement Results

The 1350 µm x 1080 µm sized AMUX chip is fabricated in ST Microelectronic's 55 nm BiCMOS technology (f_T = 325 GHz, f_{max} = 375 GHz) and consumes 380 mA at a single supply voltage of −5.7 V. Fig. 6a shows the bondwire assembly of the 2:1 AMUX chip in the RF-module of Fig. 6b. The performance of the AMUX is demonstrated by the measurement setup in Fig. 7, that consists of a Keysight DCA-X N1000a sampling scope, a Keysight E8257D signal generator and an 8-bit MICRAM DAC5 AWG, with an ENoB shown in Fig. 8, to drive the input signal channels of the AMUX RF-module. Figs. 8a,b show the measurement results at 100 GS/s

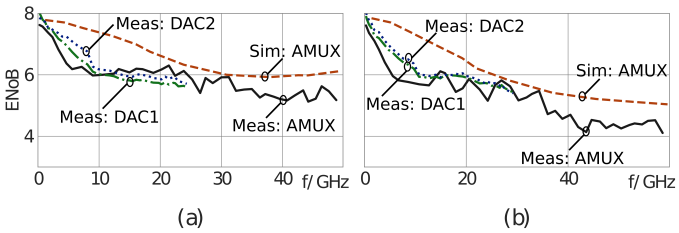

Fig. 8: ENoB measurement and simulation results of the AMUX and DAC1,2 at (a) 100 GS/s and (b) 120 GS/s.

and 120 GS/s in comparison with the simulated AMUX and the DAC1,2 input signals. The ENoB of the AMUX starts at 7.7 bit and drops down to 5.1 bit at 48.8 GHz and to 4.1 bit at 58.6 GHz, at 100 GS/s and 120 GS/s, respectively. According to the state-of-the-art presented in section I, this is the highest linearity reported for an AMUX in any kind of semiconductor technology. The DAC1,2 ENoB in Fig. 8 shows a significant drop from 8 to 6 bit already in the frequency range below 10 GHz, that is mapped by the mixers into the lower and upper AMUX bands. The simulation with the ideal 8-bit DAC1,2 signals shows in comparison only a moderate slope, that results from the original DAC1,2 frequency responses, which were considered in the simulation. The ENoB degradation from 100 GS/s to 120 GS/s in Fig. 8 is due to the high capacitive loading of the final clock buffer by the CS-transistors of the SEL stage. This results in a reduced clock signal swing whereby the signal frequency power at higher frequencies is reduced.

Fig. 9 shows the AMUX output for PAM-4 signals at symbol- and sampling rates of 64 GBd/64 GS/s, 100 GBd/100 GS/s and 120 GBd/120 GS/s as well as for a PAM-8 signal at 64 GBd/64 GS/s without pre-filtering of the DAC1,2 input signals at a differential output voltage swing of 700 mV. Compared to the state-of-the-art detailed in section I, these results represent the highest sampling- and symbol-rates reported for SiGe-technology.

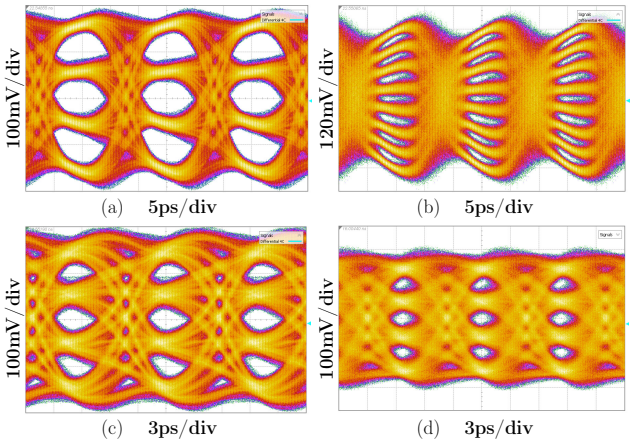

Fig. 9: Differentially measured eyediagrams at a) 64 GBd/64 GS/s PAM-4, b) 64 GBd/64 GS/s PAM-8, c) 100 GBd/100 GS/s PAM-4, d) 120 GBd/120 GS/s PAM-4.

Conclusion

In this work we have demonstrated the feasibility to double the Nyquist bandwidth of two 8-bit DACs by an AMUX circuit in SiGe-BiCMOS technology up to a record sampling rate for this kind of technology of 120 GS/s. The AMUX performance was demonstrated by 120 GBd PAM-4 and 64 GBd PAM-8 signals at 120 and 64 GS/s, respectively. Furthermore, we presented an explanatory frequency domain linearity-model for the AMUX, that explains the different characteristics of clock-duty-cycle and clock-delay based ENoB degradations. By carefully balancing the signal- and in particular the clock-path the AMUX ENoB starts with 7.7 bit at low frequencies and reaches 5.1 bit at 48.8 GHz and 4.1 bit at 58.6 GHz for sampling rates of 100 GS/s and 120 GS/s, respectively. These numbers represent the highest linearity reported for an AMUX in any kind of semiconductor technology.

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